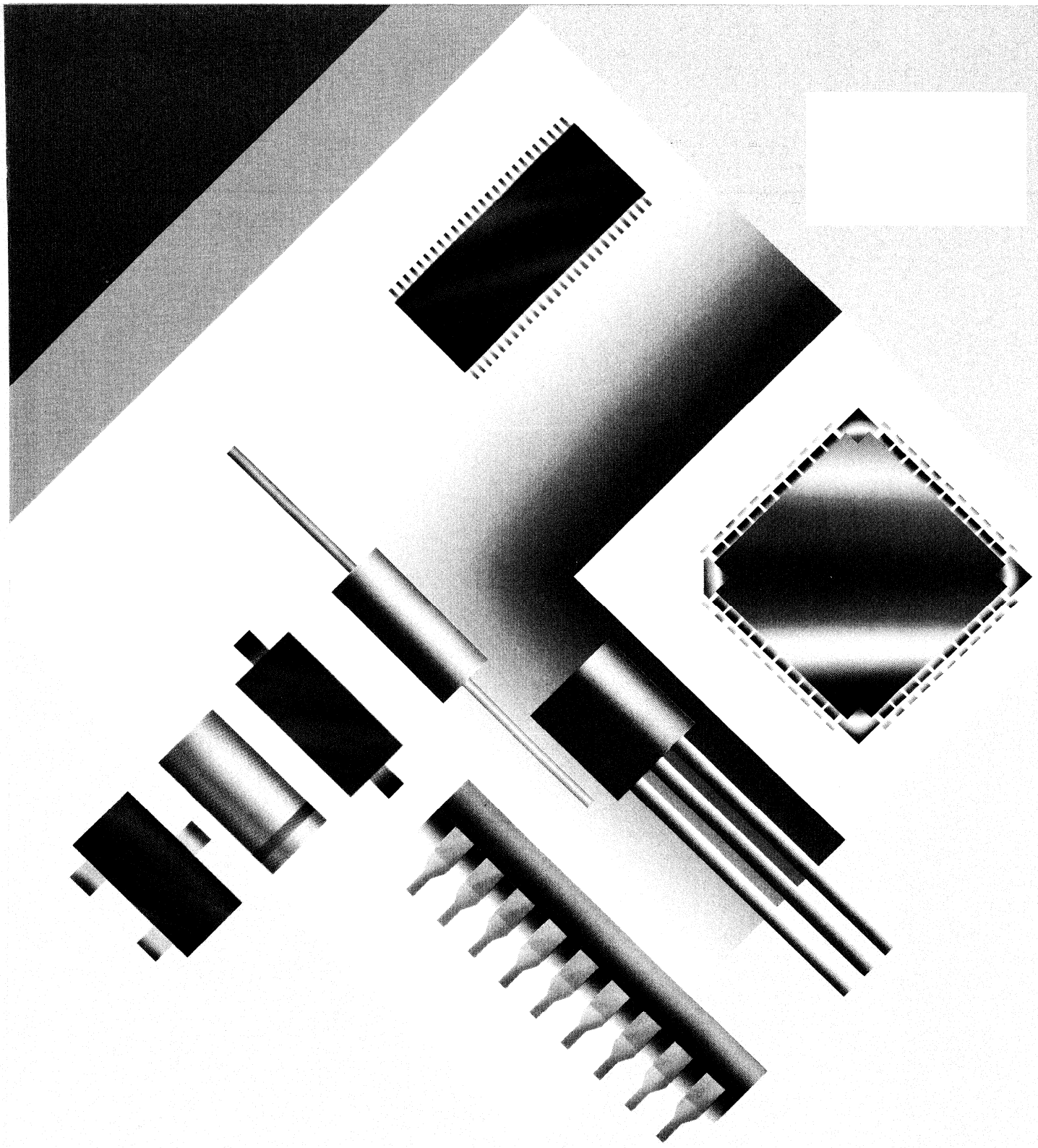

# Semiconductor Summary 1990

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ITT Semiconductors ITT

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# LIST OF TYPES

## Digital TV System

The highly integrated circuits introduced and described in brief on the following pages are components of the **all-digital color television concept "DIGIT2000"** from ITT Semiconductors. This IC set is the world's first (and still the only) television system in which picture, sound and text are all processed digitally. Since its introduction to the market in 1983, the system has been continuously refined and perfected and has reached a high level of sophistication. Today, more than 17 million TV sets worldwide have already been equipped with DIGIT2000 ICs.

### Prepared for future developments

DIGIT2000 is capable of processing signals in all present and future TV broadcasting standards: PAL, SECAM, NTSC, C-MAC, D-MAC, D2-MAC and NICAM – received via aerial, cable or satellite. Furthermore, the system guarantees upward compatibility with HD-MAC, the high-definition TV (*HDTV*) standard of the 'nineties. Thanks to its completely digital conception, DIGIT2000 is being acknowledged more and more as the technical standard of the future. That's because only digital technology guarantees **compatibility with all future developments**, whether in terms of improvements in quality or new features. Even today, it is already possible to implement some additional **features** that have only existed in theory up to now. Furthermore, significant **improvements in picture quality** are possible with various systems, especially with adaptive comb filter algorithms, intermediate storage facilities and automatic ghost compensation, which are not feasible at all with conventional analog technology.

### A flexible and programmable "kit"

In addition to these benefits, digital signal processing offers TV set manufacturers a whole range of **practical advantages**, too. To start with, digital circuits are tolerance-free and are not subject to drift or ageing phenomena. This considerably simplifies factory alignment of the sets and even permits **fully automated, computer-controlled alignment.**

Second: DIGIT2000 components are **programmable**. This means that the level of user convenience and the set's capabilities or features can be tailored to the manufacturer's individual requirements via the software.

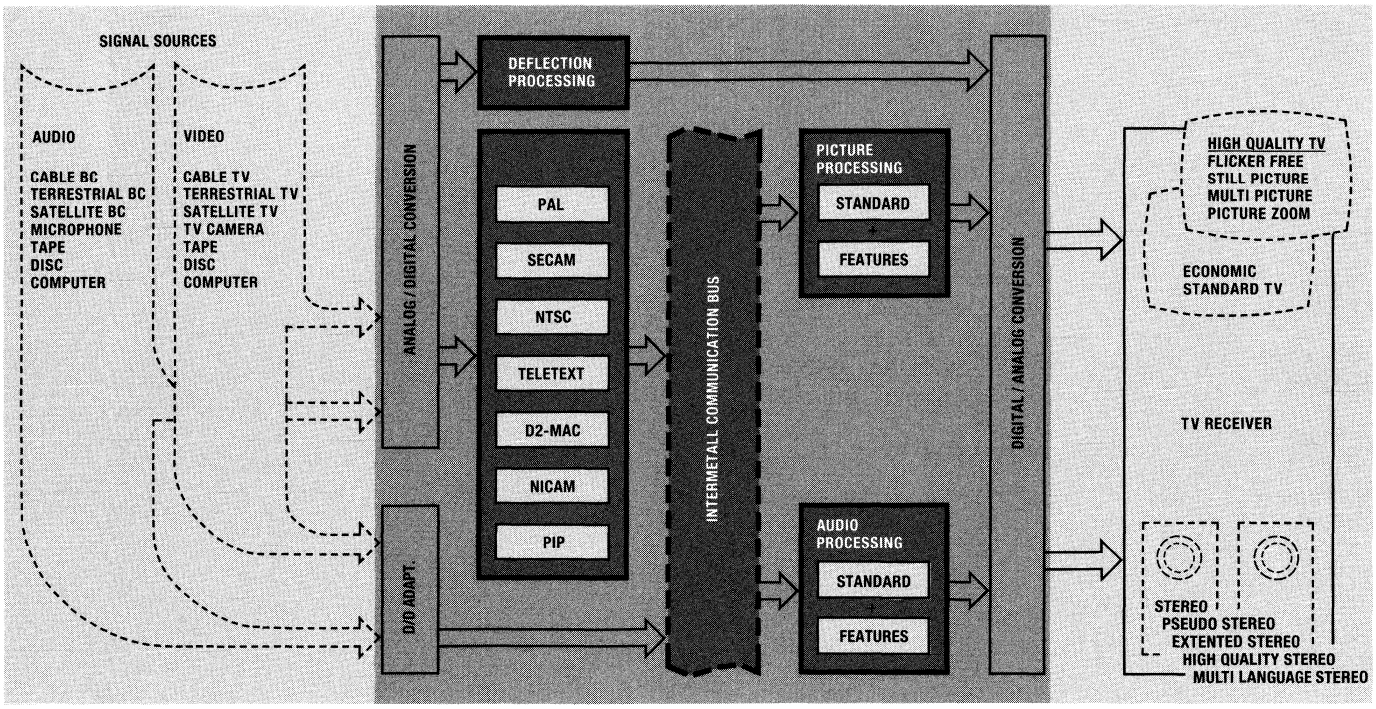
Third: DIGIT2000 is a **modular** system with a **standard circuit architecture**. All the ICs of the system are compatible with each other so that TV models of **various specifications** can be realized. These range from the low-cost standard set to the high-performance all-features multi-standard satellite receiver incorporating a host of special functions – Figure 1 gives an overview of the various possibilities which DIGIT2000 offers..

### Fully automated set manufacture

Modular construction with a handful of VLSI components and little external circuitry means that set assembly can be **fully automated**, too. Together with automatic alignment, the production process can be greatly simplified and accelerated in this way. In fact, the "insides" of digital sets look very simple and "tidy".

As figure 2 shows, the modular design of DIGIT2000 is reflected in the subdivision of the system into **functional blocks** on different levels, each of which has its own data bus structure (more about this below).

**Fig. 1:** Overview of possible DIGIT2000 Realizations




Signals of any existing or future signal source, analog or digital, can be processed: the video, audio and text processing units can handle all transmission standards.

All processing is coordinated centrally by an 8 bit microcontroller via the IM Communication Bus.

The flexibility of the modular construction permits the realization of standard TV sets as well as the gradual extension to high quality TV. The highest level of integration contains several improvements and features which cannot be realized easily with conventional analog techniques.

**Fig. 2:**
Block Diagram of the DIGIT2000 System

Basic ICs for the realization of standard TV sets

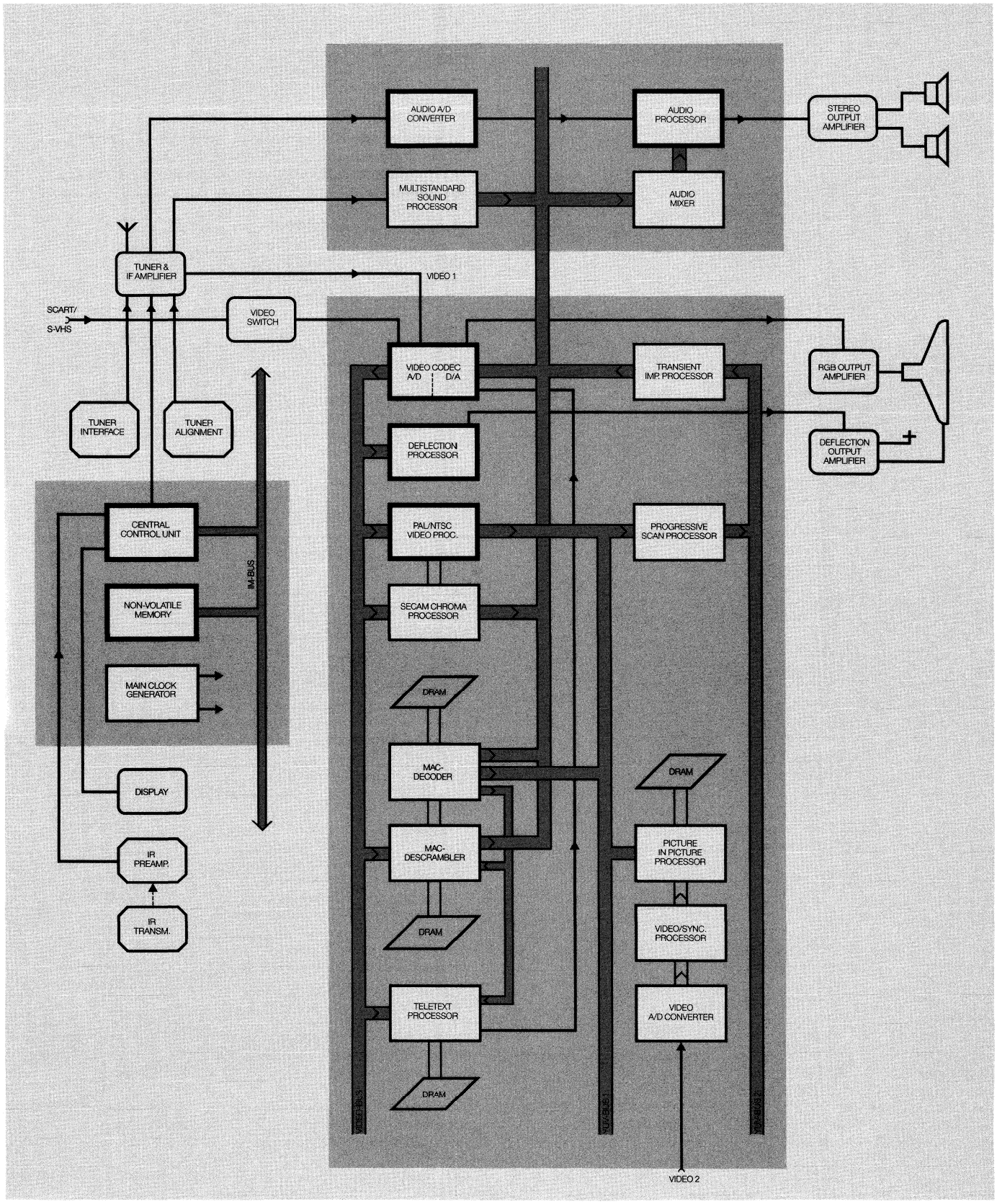
Extension ICs for the integration of quality improvements and additional features

Peripheric ICs

Components not in ITT production

Standard Dynamic Memory ICs

Data buses



**Five groups of components**

*1. Central Control Units (CCUs)*

All the signal processing components of the DIGIT2000 system are controlled by a **central 8-bit microcomputer** (the *Central Control Units, CCUs*) via the bi-directional *IM bus*. This arrangement of the ICs around a central bus makes it possible to expand the system constantly and thereby add on further improvements in the picture, sound and text processing as well as new features. The CCU is linked to a non-volatile memory in which the factory settings are stored. These are continuously compared with the present settings; in this way, it is even possible to correct deviations that are due to voltage and temperature fluctuations as well as those due to ageing phenomena in the analog components. As a result, for example, **the picture quality remains unchanged for the whole lifetime of the set.**

At present, ten different controller ICs are available which differ mainly in terms of the manner and scope of their programmability:

| | |
|---|---|
| – CCU2030 | **Central Control Unit** |
| | (with 6.8 KByte ROM) |
| – CCU2050 | (with 8 KByte ROM) |
| – CCU2070 | (with 16 KByte ROM) |
| – CCU2050PI | (with programmable remote |
| – CCU2070PI | control decoder) |
| – CCU3000 | **New generation CCU** |
| – CCU3001 | (with 32 KByte ROM) |
| – CCU3002 | (with text representation in three-layer window technique) |
| – TFPO2065 | **Tuning Processor** |
| | (with on-screen display and frequency synthesis) |
| – TVPO2066 | (with voltage synthesis) |

*2. Standard Video ICs*

The video processing section has two internal bus systems: the video bus (7 bit parallel) which carries the composite video signal from the A/D section of the video codec to the individual processors, and the YUV bus which passes on the resulting luminance and chrominance signal (8 + 8 bit parallel on 12 lines in time-division multiplex ) for further processing in the picture improvement ICs PSP and DTI (see paragraph on feature ICs) or direct to the A/D section of the video codec.

The following standard ICs are available:

| | |
|---|---|
| – PVPU2203 | **Video Processor** |
| – PVPU2204 | (for S-VHS) |
| – VCU2133 | **Video Codec** |
| – VCU2134 | (for double-scan NTSC) |
| – VCU2136 | (for S-VHS) |
| – DPU2553 | **Deflection Processor** |
| – DPU2554 | (for NTSC with progressive scan) |
| – SPU2220 | **SECAM Chroma Processor** |
| – SPU2221 | (with modified color saturation) |
| – SPU2243 | (for S-VHS) |
| – VSP2860 | **Video/Sync Processor** |
| | (including S-VHS) |
| – VAD2150 | **Video A/D Converter** |
| – VAD2170 | (for S-VHS) |

Notice that quality improvements like the **new video recording standards S-VHS and ED-Beta** or Double-scan (for NTSC) can be provided by the choice of the corresponding ICs. Several other improvement circuits will be introduced below as *Feature ICs*, among these the **comb filter processors** (ACVP, CVPU) which may be used instead or in addition to the PVPU.

*3. Standard Audio ICs*

The digital concept facilitates the processing of the new digital sound broadcasting standards as well as the input of external signal sources, such as *Digital Audio Tape* (DAT) and *Compact Disc* (CD).

Mono, stereo and multi-lingual broadcasts are automatically recognized through the software and processed accordingly. Here, the high resolution of the A/D-D/A converters permits sound quality on a par with CD (assuming digital transmission – see comments on NICAM and MAC below). The data transfer between the components of the audio section takes place via the *S bus* which, in particular, has the task of connecting the digital audio outputs of the MAC and NICAM decoders with the audio mixer AMU2481 and the audio processor APU2471. It transmits the audio information in 64-bit frames which are divided into a series of four 16-bit samples in accordance with the four audio channels.

One of this year's newcomers, the **audio processor** ACP2371, offers on one chip the functions of the A/D-D/A converters and those of a powerful, programmable signal processor and is therefore capable of carrying out the complete audio signal processing in the baseband.

Available are the following standard ICs:

| | |
|---|---|
| – ADC2301E | **Audio A/D Converter** |
| – ADC2311E | (with preemphasis) |
| – ADC2320U | (for U.S.A.) |
| – AMU2481 | **Audio Mixer** |
| | (for the processing of digital MAC or NICAM audio signals) |
| – APU2471 | **Audio Processor** |
| – APU2421U | (for U.S.A.) |
| – ACP2371 | (with A/D-D/A converters on chip) |

With the **Multistandard audio processor** (MSP) introduced in the next paragraph, the audio processing can be designed to accomodate multi-standard. This is because MSP processes not only the new digital NICAM Hifi sound standards, but also all the analog standards currently in use throughout Europe.

*4. Feature ICs*

With the DIGIT2000 system it is possible to implement a whole host of interesting features – many of them simply by fitting a single additional IC. The established television standards PAL, SECAM and NTSC are part of the standard specification of a DIGIT2000 receiver. When it comes to receiving the new MAC satllite standards and the new NICAM audio broadcasting standards with digital sound, a **D2-MAC** or a **Multi-MAC decoder/descrambler** chip set (DMA) and a **Multistandard sound processor** (MSP) are required, respectively. Substantial improvements in picture and sound can be achieved: for instance, the D2-MAC broadcasting standard offers stereo sound in CD quality or the transmission of sound commentaries in up to eight languages simultaneously.

Remarkable improvements in picture quality and innovative features can also be realized for the existing video standards by means of intermediate storage techniques: working on this basis, the newly developed **Adaptive comb filter processor** ACVP2205 is capable to eliminate almost completely the familiar cross-talk interferences between the color and brightness components (*cross-color* and *cross-luminance*) of the video signal without producing other phenomena such as "hanging dots". The resulting PAL and NTSC pictures have S-VHS quality.

Another line storage circuit is the **Progressive scan processor** (PSP) for line frequency doubling with NTSC (**Double Scan**), which "smoothens" the visible line structure of NTSC pictures.

Clearer color separation is achivied with the **Digital chroma transient improvement processor** (DTI). The latest version of this (the DTI2250) offers an additional special feature: It can represent televi-

sion pictures broadcast in the conventional 4:3 aspect ratio free from distortion on the new 16:9 format HDTV picture tubes. The inverse format conversion from 16:9 to 4:3 ("Panning") is done by the Multi-MAC descrambler DMA2285. Therefore, along with the DTI2250, a chip set is available for processing **all picture formats** – an important step on the way of compatible transition to HDTV.

Another interesting feature is the facility for inserting a second (small) picture from another program or from an external source in the main picture. All that is needed to realize this **picture-in-picture** facility is a PIP IC and a few other components.

Last but not least, there are the digital **text and graphics processors** (TPUs). These can not only process and display **teletext** in all the world's television and teletext (TTX) standards, they also permit implementation of a **menu-controlled user guidance system** and a **"service mode"** with text displays on the screen which facilitate both operation and servicing of the increasingly complex TV sets. The TPUs are also suitable, of course, for processing text and graphics from external signal sources (e.g. from personal computers). As far as teletext transmissions are concerned, the TPU recognizes the broadcast standard and language and automatically selects the appropriate character set for representation on-screen.

Available are the following feature ICs:

- DMA2271 **D2-MAC Decoder**
- DMA2275 **D2-MAC Descrambler**

- DMA2280 **Multi-MAC Decoder**
- DMA2285 **Multi-MAC Descrambler**

- MSP2400 **Multistandard Sound Processor**

- ACVP2205 **Adaptive Comb Filter Video Processor**
- CVPU2270 **NTSC Comb Filter Video Processor** (for double-scan and/or S-VHS)

- PSP2210 **Progressive Scan Processor**

- DTI2223 **Digital Transient Improvement Processor**
- DTI2250 (including picture compression function)

- TPU2735 **Teletext Processor** (for PAL/NTSC/D2-MAC, TTX level 1.5, FLOF, TOP)
- TPU2740 Multistandard TPU
- PVT2710 **Videotext and Teletext Processor**

- PIP2250 **Picture-in-picture Processor**

*5. Peripheral ICs*

The following list contains some additional ICs like clock generators (MCUs), memories (MDA, NVM), remote control transmitters (IRTs, SAAs) etc.:

- MCU2600 **Clock Generator**
- MCU2632 (for Double-scan)

- MDA2062 **1024 bit EEPROM**
- NVM3060 4096 bit EEPROM

- TFIR6400 **Tap Programmable FIR Filter**

- IRT1250 **Remote-Control Transmitter**
- IRT1260 **Remote-Control Transmitter**
- SAA1250 **Remote-Control Transmitter**
- SAA1293A Remote Control and Tuning Microcomputer

- TBA2800 **Infrared Preamplifier**

- MEA2050 **D/A and Bus Converter for IM Bus**

- MEA2901 **Tuner Interface IC**

**Forward-looking technology**

It is clear from all this that DIGIT2000 will not only keep pace with, but will play a major part in shaping the future development of television. Its kit-like structure and programmable flexibililty allows new standards and desirable features to be integrated into the system with ease. Current developments prove this: With Multi-MAC and variable aspect ratio (DMA2285 + DTI2250), the first steps have been taken towards the high definition wide-format television of the future; the adaptive comb filter has made a significant contribution to the improvement of present television pictures; the MSP2400 gives the NICAM audio system access to the TV set and, at the same time, accomodates a wide range of existing audio standards, too.

Another development objective has been to simplify TV set construction. Here, highly integrated solutions such as the one-chip audio processor ACP2371 or, available in the near future, the complete multistandard receiver on one chip, demonstrate the possibilities that are opened up by digital television technology.

ITT Semiconductors has, today, the modern technology without which such ambitious projects could not be realized. TV sets of numerous brands (more than 30) are already equipped with DIGIT 2000 ICs on all five continents. And manufacturers throughout the world can rely on the continuous support and assistance of ITT Semiconductors' own design centers in Europe, the USA and the Far East.

On the following pages each of the DIGIT2000 ICs listed above will be introduced by a short description of its basic characteristics.

## **Central Control Units** (40-Pin Plastic Package or 44-Pin PLCC Package)

These devices are 8-bit one-chip microcomputers, different in their ROM and RAM capacity:

**CCU2030** – 6.5 K Byte ROM and 120 Byte RAM
**CCU2050** – 8 K Byte ROM and 256 Byte RAM
**CCU2070** – 16 K Byte ROM and 256 Byte RAM

These types are the unprogrammed versions and are programmed during production according to the customer's specifications. For programming, an emulator board is available. The programmed versions have the type designations CCU2031, CCU2032 and so on. Combined with peripheral hardware, CCU2030, CCU2050 and CCU2070 offer the following features:

- infrared remote control
- front-panel control with up to 32 commands
- tuning by frequency synthesis (PLL) and band switching
- non-volatile program storage
- LED display for channel indication, max. 4 digits, directly driven
- storage of alignment information during production
- generation and recognition of various signals
- control of the digital signal processors for video, audio, Teletext and deflection via a serial bus (IM bus)

**CCU2050PI, CCU2070PI**

As a special feature, these versions of the CCU2050 and CCU2070 have a programmable remote-control decoder which enables matching to any infrared remote-control system on the market. By program mask, it is possible to adapt the decoder to the respective requirements. All other specifications of these CCUs are as with the basic types.

## **Central Control Units** (68-Pin PLCC Package)

CCU3000 and CCU3001 are microcontrollers in CMOS technology constructed especially for use in television sets and based on the 65C02 microprocessor. The considerable processing speed (CCU 3000: 4 MHz, CCU3001: 8 MHz) as well as supporting hardware implementations on chip (Interrupt Controller, Watchdog, Timer) result in the excellent performance of the CCU3000/CCU3001. The ROM of 1.3 kByte, provided with a stand-by option is also capable of more complex operations. The CCU3001 is equipped with a supplemental 32 kByte ROM, whereas the CCU3000 does not have an integrated ROM. External memories can replace or complement the internal memory. The 64 kByte limit of the CPU can be overcome by banking with the help of a software package. The number of banks is practically unlimited (up to 255), so that even very complex programs are feasible. The size of each bank (32 kByte) ascertains that the programming as well as the running time are hardly impeded. Both CCUs possess a programmable clock system, which enables the use of slower, external memory blocks. Besides the current consumption in the stand-by mode can be greatly reduced.

Two identical, but independent IM-bus interfaces make the connection to the processors of the DIGIT system. They are programmable up to 1 MBit/s and possess multimaster facilities. This makes it possible to realize several CCUs at the same bus. The exchange of data amongst these is enabled by 3 slave registers with which every IM-bus interface is equipped. Finally 26 (CCU3000) respectively 51 (CCU 3001) port lines are available.

Features:

- 65C02 CPU with 4 MHz (CCU3001: 8 MHz) clock
- 1344 Bytes internal RAM with stand-by
- 32 kByte ROM (CCU3001 only)
- 8 level, very fast interrupt controller
- 3 multifunctional timers
- watchdog
- 2 multimaster IM-bus interfaces of up to 1 MBit/s
- programmable clock generator with sleep mode
- on chip power-on, stand-by and clock supervision logic
- 26 (CCU3000), 51 (CCU3001) port lines
- no emulation chip necessary
- Assembler or "C" programmable

## **Central Control Unit** (40-Pin Plastic Package or 44-Pin PLCC Package)

The CCU3002 is a microcontroller constructed in CMOS technology and based on the 65C02 microprocessor, especially for use in analog television sets, but also suited for use in digital sets. A 16 kByte RAM is integrated as a memory. External memories can replace or complement the internal memory. The programmable clock generator, the IM-bus interface and the watchdog were copied from the CCU3000/3001. For the control of the TV set 5 D/A-converters with a resolution of 6 bits are available. For radiation reasons these converters are implemented statically and have ±1 mA output stages. The sixth converter has 16-bit resolution and is realized semi-dynamically at ±1 mA output current also. An analog volume control, which can be set digitally in 63 steps of 1.5 dB, can be activated instead of two of the 5 D/A converters. A preset timer (4 ms at 8 MHz) with a capture register for IR-decoding via software is available as an independent time basis.

The integrated OSD system is especially effective. There are three different layers, which may overlap and are independent from each other. Each layer can fill the complete screen. The fonts can be defined and controlled. Italics, flash, underline and transparent are selectable functions, as well as 8 foreground and 8 background colors. Softscroll up and down for each separate layer improves the readability of longer texts. The amount of software required for the control is very small, as no text has to be transported through the CPU. Font size is switchable from 8×8 to 13×8, the pixel frequeny being set by the system clock (6 to 8 MHz). Coupling of the display clock with the line frequency also takes place internally. Pixel graphics with approx. 8000 pixels are selectable, as well as the shadow effect, which improves the distinction of the separate layers. The IRQ input of the CPU can be switched to the timer, to a port line or to the horizontal, respectively vertical input of the OSD. Manipulations of the OSD can thus be effected synchroneously to the display. Text, font or graphics manipulations are possible at any time via the CPU, without disturbing the display.

Features:

- CPU with 8 MHz clock
- 1344 Bytes internal RAM
- 16 kByte ROM
- watchdog
- 5 static D/A, 6 bits with ±1 mA, 16 bit halfstatic D/A
- analog volume control on chip
- 24-bit timer
- powerful on-screen display on chip
- multimaster IM-bus interface of up to 1MBit/s
- programmable clock generator
- on chip power on, up to 21 port lines
- no emulation chip necessary
- Assembler or "C" programmable

**Central Control Units or Tuning Processors with On-Screen Display for TV Receivers** (40-Pin Plastic Package or 44-Pin PLCC Package)

These types are 8-bit one-chip microcomputers, based on the 8048, with 10 K Byte ROM and 256 Byte RAM. They are produced in N-channel MOS technology.

Depending on the programming during production according to the customer's requirements, both types can be used either as central control units in digital TV sets (DIGIT2000), similar to the CCU2030, CCU2050 and CCU2070 types, or as remote-control and tuning microcomputers for analog TV sets (similar to the SAA1293A).

The TFPO2065 or the TVPO2066 is the unprogrammed basic type and is programmed during production according to the customer's specifications. The programmed versions have the type designations TVPO2066-A23, TVPO2066-D01.

TFPO2065 and TVPO2066 offer a variety of very economic solutions for infrared remote-control, channel selection, control of analog values and on-screen display of several informations in modern CTV receivers. Additionally, in the case of use as CCU, they control the several digital signal processors which form the DIGIT2000 system. In the case of **TFPO2065**, tuning is done by frequency synthesis (PLL), and in the case of the **TVPO2066** by voltage synthesis (rate multiplier). All other features of these two devices are identical, so that they can be described together.

In conjunction with the SAA1250, IRT1250 or IRT1260 Remote-Control Transmitter, the TBA2800 Infrared Preamplifier and the MDA2062 or NVM3060 Non-Volatile Memories, a complete control section of a CTV receiver can be designed. Many features of this can be varied by software, so manufacturers are able to realize their own ideas to a large extent.

The integrated on-screen display facility offers two lines of five characters each. The character set includes 32 characters, which are ROM-defined. A character is made up of a dot matrix of 5 times 7 dots. Fringing and rounding functions are fully available, and fringe color as well as background color can be set. Display duration can also be selected. No external components are required for synchronizing the display with the main picture. Possible indications are, for example:

| | |
|---|---|
| P 12 | for program 12 or memory location 12 |
| C 28 | for channel 28 |
| VOL 15 | for volume, 15$^{th}$ position |
| SAT 3 | for color saturation, 3$^{rd}$ position |
| 29 | for 29 minutes of sleep time |
| 12 : 38 | for time in case of real-time clock function |

**Features**

- infrared remote-control decoder
- four 6-bit D/A converters
- programmable divider for frequency synthesis with TFPO2065
- 12-bit rate multiplier for voltage synthesis with TVPO2066
- IM bus interface for serial communication with the MDA2062 or NVM3060 Non-Volatile Memories and with the other DIGIT2000 processors
- Port P2 and P3 for universal input/output functions, e.g. keyboard, bandswitch, multistandard switch, VCR switch, AFC, etc.
- mains flip-flop for standby mode
- built-in on-screen display facility via RGB outputs

**Video Codecs** (40-Pin Plastic Package or 44-Pin PLCC Package)

High-speed coder/decoder ICs in CI technology for analog-to-digital and digital-to-analog conversion of the video signal in digital TV receivers. The VCU2133 is intended for normal-scan TV receivers, also with D2-MAC, whereas the VCU2134 is designed to be used in digital TV receivers for the NTSC system and equipped with double-scan facility. With the help of two control bits the VCU2136 allows three possible operation modes: "Composite Video", "VHS" and "S-VHS".

A single silicon chip combines the following functions and circuit details:

- two input video amplifiers
- one A/D converter for the composite video signal (FBAS) of the flash type
- one D/A converter for the luminance signal
- two D/A converters for the color difference signals
- one RGB matrix for converting the color difference signals and the luminance signal into RGB signals
- three RGB output amplifiers
- programmable auxiliary circuits for blanking, brightness adjustment and picture tube alignment
- inputs for text signals
- beam current limiting

## **Video Processors** (40-Pin Plastic Package or 44-Pin PLCC Package)

The PVPU2203 is a digital real-time signal processor for processing the video signals digitized by the VCU2133 Video Codec in digital color TV receivers. The PVPU2204 together with the VCU2136 is additionally capable for S-VHS operation mode.

Both video processors are N-channel MOS circuits and contain on a single silicon chip the following functions:
- a code converter
- the chroma bandpass filter
- the chroma trap with peaking facility
- a contrast multiplier with limiter for the luminance signal
- all color signal processing circuits such as automatic color control (ACC), color killer, PAL identification, decoder with PAL compensation or NTSC comb filter, phase comparator, hue correction, etc.
- a color saturation multiplier with multiplexer for the color difference signals
- the IM bus interface circuit for communicating with the CCU2030, CCU2050, CCU2070 or CCU3000 Central Control Unit
- circuitry for measuring dark current (CRT spot-cutoff), white level and photo current, and for transferring this data to the appropriate Video Codec

## **Adaptive Comb Filter Video Processor** (40-Pin Plastic Package or 44-Pin PLCC Package)

Digital real-time video processor for multistandard color TV sets based on the DIGIT2000 system. In combination with the VCU2136 the ACVP2205 is additionally capable of the S-VHS mode operation. It is designed in N-MOS technology.

The ACVP2205 is equipped with an adaptive 2H combfilter which gives a perfect luma/chroma separation to improve the resolution. Due to the adaptive processing, no artifacts such as "cross color, cross luminance, sitting or hanging dots" are visible. In PAL the full vertical resolution is now available.

A second facility of the ACVP2205 is an adjustable black level expansion to improve the picture contrast and the gamma-correction, especially with large displays. An adjustable vertical peaking enhances the vertical resolution.

The ACVP2205 includes all functions of the PVPU2204 and is fully pin- and software-compatible. The main features are:
- 2H adaptive combfilter
- luminance contrast multiplier and horizontal peaking
- adjustable black level expansion
- vertical peaking
- all color signal processing, such as decoder, ACC, color killer, phase comparator, hue correction, saturation multiplier etc.
- circuitry for CRT measurements

## **NTSC Comb Filter Video Processor for S-VHS and/or Double-Scan** (40-Pin Plastic Package or 44-Pin PLCC Package)

The CVPU2270 is a digital real-time signal processor for video signals in NTSC color TV receivers based on the DIGIT2000 concept, and equipped with S-VHS facility, also suited for double-scan horizontal deflection. It is designed in NMOS technology.

The S-VHS system provides an enhanced picture quality from video recorders as follows: When recording, the luma and chroma signals are modulated on separate carriers. At playback, they are derived separately on their respective carriers, from which they must be demodulated. Thereafter, the chroma signal is modulated on the usual color subcarrier. Hitherto, these two signals were added to produce the normal analog composite video signal which was given on one line to the SCART connector of the TV set. With S-VHS, by means of an additional connection, baseband luma and subcarrier-modulated chroma are transported, independently, from the recorder to the TV set, where they are processed further, separately. In this way, possible distortions arising from the addition of the two signals are avoided. Baseband luma and subcarrier-modulated chroma are digitized separately in the VAD2170 Video A/D Converter, and the digital luma and chroma signals multiplexed on seven lines, and fed to the CVPU2270 video processor.

A second facility of the CVPU2270, which can be used optional in addition to S-VHS, is the double-scan horizontal deflection, which provides a further increased picture quality. In normal NTSC TV receivers, only about 450 lines are shown on the screen, because 25 of the system's 525 lines are used for vertical flyback and further 50 cannot be seen due to 10% "overscan". Thus, the picture impression is relatively poor. Double-Scan provides a picture improvement by displaying each line twice, which means that about 900 lines are written. For this, the horizontal deflection is at 32 kHz, and the information for each second line is derived by storing the video information of one line in a video memory (PSP2210 Progressive Scan Processor).

The CVPU2270 contains on a single chip:
- an input demultiplexer
- two code converters
- an NTSC comb filter
- the chroma bandpass filter
- the luma filter with peaking and coring facility
- the contrast multiplier with limiter for the luma signal
- all color signal processing circuits such as automatic color control (ACC), color killer, identification, decoder and hue correction
- a color saturation multiplier with multiplexer for the color difference signals
- the IM bus interface for communicating with the CCU
- circuitry for measuring dark current and white level, and for transferring this data to the VCU

## **SECAM Chroma Processors** (40-Pin Plastic Package or 44-Pin PLCC Package)

Digital real-time signal processors for processing SECAM video chroma signals in combination with the appropriate video processors, which process the luminance information at the same time.

The SPU2220 and SPU2221 work together with the PVPU2203 Video Processor, whereas the SPU2243 works together with the PVPU2203 or PVPU2204 Video Processors. The SPU2221 and SPU2243 differ from the SPU2220 in that the color saturation multipliers were changed from ×2 to ×4, and that the SPU2243 in combination with the PVPU2204 is also suitable for S-VHS operation mode.

These SECAM Chroma Processors are N-channel MOS circuits and contain on a single silicon chip the following functions:

- a code converter
- a digital SECAM bell filter
- a switchable IF compensation filter
- a digital FM demodulator with DC offset correction, deemphasis and demultiplexer
- a digital Red-/Blue-line identification
- a digital standard recognition circuit
- a color saturation multiplier with multiplexer for the color difference signals
- tristate outputs for the color difference signals
- the IM bus interface circuit which provides the communication with the CCU2030, CCU2050, CCU2070 or CCU3000 via the IM bus.

## **Picture-in-Picture Processor** (68-Pin PLCC Package)

Picture-in-picture means the insertion of a second program's picture on the screen of a CTV receiver (at reduced size) simultaneously with the full-size main picture. The second, small picture may originate from another TV transmitter, from a video recorder, a monitor camera or another source. It allows monitoring of the second channel while watching the main channel. Main requirement for picture-in-picture is to store the content of the small picture when it is supplied by its source, and to deliver the content at the proper instant when it must be inserted into the main picture which is received and displayed continuously. For storing the content of the second, small picture, two standard 64 K dynamic RAMs (16 × 4) are used, thus making the storage simple and economic. Today's picture-in-picture fits neatly into the well-known DIGIT2000 system, but is also suitable for stand-alone applications.

The PIP2250 is a fast signal processor in CMOS technology which is used to filter (for anti-aliasing) and to decimate the digital Y, R–Y and B–Y signal supplied by the VSP2860 Video/Sync Processor, to control the DRAMs for storing the small picture's content and for reading the same at the proper time for display. Further, a border generator supplies the borderline for the small picture.

## **Video A/D Converter** (18-Pin Plastic Package or 44-Pin PLCC Package)

The VAD2150 is a fast 7-bit A/D converter of the flash type, designed in CI technology. It consists mainly of 127 fast comparators and is primarily intended for the A/D conversion of the video signal for the second channel in the picture-in-picture system, based on the DIGIT 2000 digital TV concept. In this application, the VAD2150 acts together with the VSP2860 Video/Sync Processor and the PIP2250 Picture-in-Picture Processor. The VAD2150 may also be used in other applications which call for a low-cost high-speed A/D converter, such as TV scramblers, Teletext decoders, video memory applications, DBS satellite receivers using a MAC TV system, etc.

Main features of the VAD2150 Video A/D Converter are:

- no external sample and hold required
- high-speed operation: 25 MHz
- output word Gray coded
- two inputs with different input amplitude can be selected
- gain of the input amplifiers can be doubled

## **Video A/D Converter for S-VHS** (18-Pin Plastic Package or 44-Pin PLCC Package)

The VAD2170 is a fast 7-bit A/D converter of the flash type, manufactured in CI technology (CI = collector implanted). It mainly consists of 127 fast comparators and is primarily intended for the A/D conversion of the luma and the chroma signal in NTSC color TV receivers according to the DIGIT2000 system and equipped with the S-VHS facility, which in detail is described in the data sheet of the CVPU2270 Comb Filter Video Processor for S-VHS and/or Double-Scan. The VAD2170 can also be used in other applications which call for a low-cost high-speed A/D converter, such as TV scramblers, digital Teletext decoders, video memory applications, D2-MAC DBS satellite receivers etc.

**Features**

- 7-bit flash A/D conversion
- no external sample and hold required
- high-speed operation: 20 MHz
- full compatability with the DIGIT2000 system
- multiplexed luma and chroma output words, Gray-coded
- two analog inputs for separate input of luma and chroma
- two different operation modes selectable

## **Video/Sync Processor** (40-Pin Plastic Package or 44-Pin PLCC Package)

The VSP2860 is a digital signal processor in NMOS technology, which is able to cover all functions of digital signal processing in the video and sync section of a digital TV receiver which are normally combined in the VPU and DPU processors and the MCU clock generator of the DIGIT2000 digital TV system. The VSP2860 is intended for the second video channel in digital TV receivers equipped with the picture-in-picture facility.

Main features of the VSP2860 Video/Sync Processor are:
- luma channel with delay compensation, color trap, peaking filter, contrast multiplier and limiter
- chroma channel with color demodulator, ACC, color killer, color saturation multiplier, limiter and chroma multiplexer
- user-adjustment of contrast, color saturation, hue etc.
- sync separation section with sync slicer, horizontal PLL, vertical separation, vertical counter, horizontal decoder and vertical decoder, output pulse generation
- clock generation on-chip, or external clock

## **MAC Decoders** (68-Pin PLCC Package)

In order to receive TV channels transmitted via satellite, using the newly established D2-, D-, or C-MAC standards instead of PAL or SECAM, decoders are required for decoding the TV video and sound signals. The DMA2271 and DMA2280 are suitable for this purpose in conjunction with the DIGIT2000 digital TV system and also for stand-alone solutions.

The DMA2271 is only able to decode D2-MAC/Packet signals, in contrast to the DMA2280 which decodes D2-, D-, or C-MAC/Packet Signals.

The DMA2271/2280 process the D2-, D- or C-MAC baseband signals which have been digitized by the VCU2133 Video Codec Unit using a sampling frequency of 20.25 MHz. For time expansion, the video samples of each line are stored in a RAM which is on-chip, and read at the lower rate of 13.5 MHz for the luminance and 6.75 MHz for the color difference signals. An interpolation from 13.5 MHz to 20.25 MHz is performed in order to overcome the need for a second clock of 13.5 MHz and to simplify the reconstruction filters placed after the D/A conversion (RGB outputs of the VCU).

The digital video filters contained in the DMA2271/2280 are switchable, and the error correction logic of the sound/data part is used to detect the bit-error rate. So it is possible to control the luma and chroma bandwidth depending on the noise contained in the input signal.

The DMA2271 is able to process duobinary coded signals with a bit rate of 10.125 Mbit per second and the DMA2280 with a bit rate of 20.25 Mbit per second out of one subframe.

For sound and data processing the duobinary-coded signal is filtered and sliced very carefully to achieve a low bit-error rate. The DMA2271/2280 can process all 16 possible configurations and up to four channels in parallel and uses all possibilities to detect and correct errors. The time expansion of the sound samples is achieved by buffering the corrected samples in an external DRAM and reading them at a rate of 32 kHz.

The digital sound signals are supplied by the DMA2271/2280 via the so-called Sound bus (S-Clock, S-Ident and S-Data) in a serial format. In the case of a DIGIT2000 TV receiver, they are further processed in the AMU2481 Audio Mixing Unit which provides filtering of the medium-quality channels and allows mixing of the four sound channels. The AMU2481's digital serial output is routed to the APU2471 Audio Processor, also via the sound bus. The APU2471 carries out functions like adjustment of volume, bass and treble, loudness etc., and provides D/A conversion for the four sound channels.

## **MAC Descrambling Processors** (68-Pin PLCC Package)

The DMA2275 is a digital real-time descrambling processor only for the D2-MAC/Packet system, whereas the DMA2285 is a digital real-time descrambling processor for the D2-, D- and C-MAC/Packet systems.

Together with the appropriate decoder chips DMA2271 (D2-MAC) or DMA2280 (D2-, D- and C-MAC), they can be used to build up a D2-, D-, or C-MAC/Packet conditional access receiver.

The programmable VLSI circuits in CMOS technology contain on a single silicon chip the following functions:

DMA2275/2285
- descrambling of MAC video signal
- interpolation of MAC video signal (aspect ratio 16:9)
- descrambling of D2-, D-, or C-MAC data packets
- descrambling of VBI-teletext
- entitlement packet aquisition
- supplementary general purpose packet acquisition
- line 625 acquisition
- communication with external microprocessor via IM bus

DMA2285 only
- one subframe sound processing

**Digital Transient Improvement Processor** (40-Pin Plastic Package or 44-Pin PLCC Package)

Color TV according to the present state of the art suffers from the limited chroma bandwidth available in the transmission system, due to the necessity to have a system which is compatible to the hitherto-used black-and-white transmission system. The luminance information is transmitted using a 4 MHz bandwidth, and for the chrominance information which is transmitted by means of a 4.433 MHz subcarrier for PAL, 3.579 MHz for NTSC, only a bandwidth of about 1 MHz is available. This leads to (partially) unsatisfactory sharpness of color transients on the screen, especially if the accompanying luminance transient is small. A considerable improvement is offered by the DTI2223 Digital Transient Improvement Processor which fits into the DIGIT2000 digital TV system almost without additional cost besides the IC itself.

Additionally to the transient improvement circuitry itself, the DTI2223 contains two delay lines which serve for compensating the delay in the luma and chroma paths of the DIGIT2000 system in such a way, that they introduce a further adjustable delay which extends the original delay, caused by the video processor, by such an amount that an overall delay of one horizontal sweep is reached. This is necessary, if analog RGB signals are fed to the VCU video codec, e.g. in the case of Antiope or Teletext.

The DTI2223 is an N-channel MOS circuit which contains on one silicon chip mainly the following functional blocks:
- adjustable luma delay line (0 to 61 $\mu$s)
- adjustable chroma delay line (0 to 61 $\mu$s)
- chroma nibble demultiplexer and R–Y/B–Y demultiplexer
- R–Y and B–Y interpolation filters
- R–Y and B–Y risetime detectors
- hold pulse generator
- chroma nibble multiplexer
- clock generator and MUX/DEMUX control
- DTI luminance delay circuit
- IM bus interface

**Digital Transient Improvement Processor** (40-Pin Plastic Package or 44-Pin PLCC Package)

The DTI2250 contains all the functions of the DTI2223 such as chroma transient improvement, chroma hue and saturation adjustment and two delay lines to compensate the luma and chroma delays.

Together with new transmission standards such as MAC, Q-PAL or I-PAL a new picture format with an aspect ratio of 16:9 has been specified. For a compatible display of a 4:3 source on a 16:9 screen an appropriate horizontal compression by 1/4 has to be carried out to ensure the proper picture geometry.

The DTI2250 incorporates an adjustable compression function that allows any horizontal picture compression from 0% (no compression) to 25% in 86 steps. It is designed in N-MOS technology and is fully pin-and software-compatible to the DTI2223. The main features are:
- adjustable luma FIFO delay line (0 to 61 $\mu$s)
- adjustable chroma FIFO delay line (0 to 61 $\mu$s)
- luma and chroma interpolation for compression
- coefficient control
- chroma interpolation and risetime detectors
- hold pulse generator
- color saturation multiplier and hue correction

**Tap Programmable FIR Filter** (68-Pin PLCC Package)

The TFIR6400 is a digital real-time signal processor that allows the flexible and fast implementation of video filters, especially for ghost compensation. In cascaded applications a large number of taps is possible. On a single chip the TFIR6400 contains a complete FIR-filter with 64 taps using fully programmable multipliers. It is designed in CMOS technology and operates with clock frequencies of up to 20.5 MHz. The following functions are implemented:

- 64 tap FIR-filter
- 8-bit data, 10 bit coefficients
- tap coefficients are programmable by parallel interface
- rounding for each multiplier output
- inputs and outputs for cascaded application
- selectable overflow detection and limitation
- recursive structures (IIR) possible
- max. 20.5 MHz clock frequency

**Progressive Scan Processor** (40-Pin Plastic Package or 44-Pin PLCC Package)

In NTSC TV receivers, only about 450 lines are normally displayed on the screen, because 25 of the system's 525 lines are used for vertical flyback, and 50 cannot be seen due to 10% "overscan". Thus, the picture impression is relatively poor.

The NTSC double-scan version of the DIGIT2000 system provides a considerable picture improvement by displaying each line twice, which means that about 900 lines are on the screen. For this, the horizontal deflection ist at 32 kHz, and the information required for each second line is derived by intermediate storage of the video information in a dual-port video memory.

The video part of one line supplied by the CVPU2270 Comb Filter Video Processor, is written into the dual-port video memory contained in the PSP2210, using the main clock rate of 14.3 MHz, while the signals of the previous line are twice read from the memory at double the clock rate. In this way, the data of one line is read twice while one line is written.

The PSP2210 is an NMOS VLSI Circuit, mainly acting as dual-port video memory in digital color TV receivers based on the DIGIT2000 concept and equipped with double-scan horizontal deflection. The device acts together with the VCU2134 Video Codec and the CVPU2270 Comb Filter Video Processor and the other processors of the DIGIT2000 system.

## **Audio A/D Converters Europe** (24-Pin Plastic Package or 44 Pin PLCC Package)

Analog-to-digital converters, improved and full compatible to the old versions ADC2300E, ADC2310E, for digitizing the analog stereo sound signals in digital TV receivers based on the DIGIT2000 system. They are intended for working together with the APU2471 Audio Processor, controlled by the CCU2030, CCU2050, CCU2070 or CCU3000 Central Control Unit and clocked by the MCU2600 or MCU2632 Clock Generator.

The ADC2301E and ADC2311E are integrated circuits in CI technology containing the following functions on one silicon chip:
- several analog input and output amplifiers
- analog switches for selecting different signal sources
- an analog stereo dematrix circuit
- a level control facility
- two pulse-density modulators (PDM1 and PDM2)
- an IM bus interface

The difference between ADC2301E and ADC2311E is the gain of the AUXin input and AUXout output. The ADC2301E is intended to be used without preemphasis at AUXin. The ADC2311E is intended to be used with preemphasis at AUXin. In order to compensate the loss of the preemphasis network the gain of the AUXin input amplifiers has been increased.

## **Audio Processor** (24-Pin Plastic Package or 44-Pin PLCC Package)

Programmable digital real-time signal processor for processing digitized sound signals. It is designed to process digital audio data either coming from an ADC2301E or ADC2311E Analog-to-Digital Converter or from the AMU2481 Audio Mixing Unit. The basic functions of the processor are mask-programmed. Coefficients for volume, bass, treble, balance, etc., can be modified by the CCU2030, CCU2050, CCU2070 or CCU3000 Central Control Unit via the serial IM bus.

The APU2471 is an N-channel MOS circuit. It contains some hardwired digital filters for converting pulse-density modulated sound signals into PCM data, a programmable DSP core and four digital-to-analog converters. The hardware blocks of the APU2471 are:
- IM bus interface; input/output interface with the IM bus
- digital decimation filters
- DAC; output interface circuit for converting the processed audio data
- Vol 2; analog volume adjustment (additional attenuation)
- C RAM 32 · 8 bits; memory for variable coefficients
- C ROM 28 · 8 bits; memory for constant coefficients
- data RAM 50 · 16 bits; memory for state variables (intermediate results) and general purpose variables
- arithmetic logic unit ALU; a fast 16 · 8 bit multiplier, adder, accumulator (20 bits) and circuit for shift operations as well as overflow logic with a saturation characteristic
- separator; separates the very fast data bus I from the slower data bus II
- program counter; loadable incrementer for addressing the program memory
- program ROM 256 · 14 bits; contains all programs (mask-programmed)
- control unit; coordinates the timing of all functions
- serial I/O; serial sound bus interface for 4 channels of 16 bit each Data-Input and Data-Output on different pins

## **Audio Processor with A/D, D/A Converters** (44-Pin PLCC Package)

One-chip replacement for the well-known ADC/APU combination with several new features. Programmable digital real-time processor for processing analog or digitized sound signals in TV receivers. Working together with the NICAM Demodulator/Decoder MSP2400 and the Audio Mixer AMU2481, you get a complete multistandard audio system controlled by the CCU2030, CCU7050, CCU2070 or CCU3000 Central Control Unit via the serial IM bus. The basic functions of the DSP processor are mask-programmed.

The A/D circuit of the ACP2371 is designed in CMOS technology, the processor part in NMOS technology. It contains some hardwired digital filters for converting pulse-density modulated sound signals into PCM data, a programmable DSP core and four digital-to-analog converters.

The functions and hardware implementations of the ACP2371 are:
- IM bus interface
- analog switches for selecting different signal sources
- additional signal input pair (AUXDIN1, AUXDIN2)
- additional signal output pair (AUXOUT1, AUXOUT2)
- automatic level control for each input channel
- additional gain adjust for TVIN2 input
- three pulse-density modulators (sigma-delta-principle)
- pilot input with separate A/D converter and identification signal decoder
- stereo dematrix circuit
- digital decimation filters
- 4 D/A converters (Main- and Aux-channels)
- analog volume adjustment for all DAC outputs (additional attenuation)
- switchable deemphasis DE1 for AUXOUT path
- serial sound bus interface; I/O for 4 channels of 16 bit
- C RAM 32 · 8 bits; memory for variable coefficients
- C RAM 28 · 8 bits; memory for constant coefficients
- data RAM 50 · 16 bits; memory for state variables (intermediate results) and general purpose variables
- arithmetic logic unit ALU; a fast 16 · 8 bit multiplier, adder, accumulator (20 bits) and circuit for shift operations as well as overflow logic with a saturation characteristic
- separator; separates the very fast data bus I from the slower data bus II
- program counter; loadable incrementer for addressing the program memory
- program ROM 256 · 14 bits; contains all programs (mask-programmed)
- control unit; coordinates the timing of all functions

**Audio Mixer** (24-Pin Plastic Package or 44-Pin PLCC Package)

Programmable digital real-time signal processor, for processing digitized sound signals. It is designed to perform digital processing of both TV audio information and digital audio data from the DMA2271 or DMA2280 D2-MAC Decoders or the MSP2400 Multistandard Sound Processor. The basic functions are mask-programmed. Coefficients determining several operation modes can be modified by the CCU2030, CCU2050, CCU2070 or CCU3000 Central Control Unit via the serial IM bus.

The AMU2481 is an N-channel MOS circuit and contains a serial/parallel converter, a parallel/serial converter, a programmable DSP core and four digital-to-analog converters.

The hardware blocks of the AMU2481 are:
- S bus interaface; serial sound bus interface for 4 channels of 16 bit each Data-Input and Output
- DAC; output interface circuit for converting the processed audio data
- IM bus interface; input interface with the IM bus
- C RAM 32 · 8 bits; memory for variable coefficients
- C ROM 28 · 8 bits; memory for constant coefficients
- data RAM 50 · 16 bits; memory for state variables (intermediate results) and general purpose variables
- arithmetic logic unit ALU; a fast 16 · 8 bit multiplier, adder, accumulator (20 bits) and circuit for shift operations as well as overflow logic with a saturation characteristic
- separator; separates the very fast data bus I from the slower data bus II
- program counter; loadable incrementer for addressing the program memory
- program ROM 256 · 14 bits; contains all programs (mask-programmed)
- control unit; coordinates the timing of all functions

**Multistandard Sound Processor** (44-Pin PLCC Package)

Since the introduction of digital sound transmission via NICAM 728 for terrestrial TV transmission in various European countries the necessity for an IC capable of multistandard performance for television audio processing has arisen. This new digital technology makes it possible to transmit two high-quality audio channels in addition to the conventional FM mono channel, using the so-called DQPSK (Differential Quadrature Phase Shift Keying). Coding (data reduction) is achieved with the Near Instantaneous Companding System (NICAM).

The MSP2400 fulfils all requirements set by European TV standards. With the help of programmable mixers and filters the MSP is capable of regaining NICAM-coded as well as FM/AM-modulated audio channels from a sound IF signal. The IC works in two selectable operation modes:
1. NICAM and FM/AM Mono
2. FM stereo

The output of the MSP2400 at the digital output pin (S-bus) provides up to 3 different audio baseband channels. Together with the ICs AMU2481 and ACP2371 an audio system is achieved which performs the complete sound processing in any TV concept. Some of the advantages of this system are:
- integrated 8-bit A/D converter
- all demodulators, NICAM decoder and filter functions are digitally integrated
- programmable mixers and filters permit the processing of sound IF signals of theoretically 0 to 9 MHz
- NICAM system selectable as standard BG or I
- no special input filters or other analog filters necessary
- only one system clock frequency
- Pay-TV in preparation

**Audio A/D Converter U.S.A** (24-Pin Plastic Package or 44-Pin PLCC Package)

Analog-to-digital converter for digitizing the analog sound signals in a digital TV receiver (DIGIT2000) with a MTS section (MTS = Multichannel Television Sound). The ADC2320U is the advanced successor of the well-known ADC2300U which has been extended by an automatic level-control facility. It is an integrated circuit in CI technology and contains the following functions on one silicon chip:
- two A/D converters of the pulse-density modulator type
- three analog switches for selecting different signal sources
- the automatic level-control facility
- the DIF synchronous AM demodulator
- the SAP FM demodulator and detector
- the IM bus interface circuit, acting as receiver for commands given by the CCU2030, CCU2050, CCU2070 or CCU3000 Central Control Unit to control the analog switches and the SAP detector, or acting as transmitter for the SAP bit sent to the CCU.

**Audio Processor U.S.A** (24-Pin Plastic Package or 44-Pin PLCC Package)

Programmable digital real-time signal processor for processing the audio signals digitized by the ADC2320U Audio A/D Converter in digital CTV receivers (DIGIT2000) to NTSC standard, equipped with a MTS section (MTS = Multichannel Television Sound). Together, ADC2320U and APU2421U comprise a complete digital multichannel sound processing system (U.S. standard).

The APU2421U is the advanced successor of the well-known APU 2400U which has been extended by the integration of the MTS processor (which replaces the hitherto-required analog expander) and a clock generator. It is an NMOS circuit and, controlled by software, carries out the following functions:
- converting the pulse-density modulated input signals into parallel data at the audio sample rate
- MTS processor which executes DIF/SAP expanding
- dematrixing
- fixed preemphasis
- bass and treble control
- stereo basewidth enlargement
- balance and volume control
- detection of the pilot subcarrier signal
- DAC; output interface circuit for converting the processed audio data into analog signals, DAC1 for Main channel, DAC2 for Aux channel

## **Deflection Processors** (40-Pin Plastic Package or 44-Pin PLCC Package)

Programmable VLSI circuits in N-channel MOS technology for carrying out the deflection functions in digital color TV receivers, also suitable for text and D2-MAC applications. The two types are basically identical, but are modified according to the intended application:

**DPU2553** – normal-scan horizontal deflection, standard CTV receivers, also equipped with Teletext and D2-MAC facility

**DPU2554** – double-scan horizontal deflection, for NTSC CTV receivers equipped with double-frequency horizontal deflection for improved picture quality

These Deflection Processors contain the following circuit functions:
- video clamping
- horizontal and vertical sync separation and synchronization
- normal and double-scan horizontal deflection
- east-west correction, also for Trinitron picture tubes
- normal and double-scan vertical deflection
- sawtooth generation
- text display mode with increased deflection frequencies (18.7 kHz horizontal and 60 Hz vertical)
- D2-MAC operation mode

## **Clock Generator ICs** (14-Pin Plastic Package)

Integrated circuits in CI technology for generating the main clock ∅M (MCU2600) and the double-scan clock ∅D (only MCU2632) for digital TV receivers according to the DIGIT2000 concept, also for those with double frequency horizontal deflection.

These Clock Generator ICs supply the digital signal processors, decoders, converters etc. of the DIGIT2000 digital TV system with the required main clock (MCU2600) and withe the main and double-scan clock signals (MCU2632). For PAL and SECAM, the clock frequency is four times the PAL color subcarrier frequency, and for NTSC, the clock frequencies are four and eight times the NTSC color subcarrier frequency:

| | |
|---|---|
| for PAL and SECAM: | $f_{\varnothing M} = 4 \times 4.433\,618\,75\ \text{MHz} = 17.734\,475\ \text{MHz}$ |
| for NTSC: | $f_{\varnothing M} = 4 \times 3.579\,545\ \text{MHz} = 14.318\,180\ \text{MHz}$ |
| | $f_{\varnothing M} = 8 \times 3.579\,545\ \text{MHz} = 28.636\,36\ \text{MHz}$ |
| for D2-MAC: | $f_{\varnothing M} = 20.25\ \text{MHz}$ |

## **Teletext Processor for Level 1 Teletext** (40-Pin Plastic Package or 44-Pin PLCC Package)

The TPU2735 is specified to handle Level-1-Teletext information (in German: Videotext). In this function, it is part of the DIGIT2000 digital TV system and works in conjunction with the other VLSI circuits and processors of this system. The Teletext adapter designed with the TPU2735 is very simple and economic, so that this new feature may now become common as it was not possible due to the high cost of former multichip solutions up to now.

The TPU2735 is a N-channel MOS circuit, and contain the following functions on a single silicon chip:
- one-chip solution of the Teletext processing (except for external RAM)
- ghost compensation to eliminate the effects of ghost pictures
- as input signal the 7-bit digitized video signal is used delivered in a parallel Gray code by the VCU Video Codecs
- reduced access time is provided for the Teletext pages by receiving and storing up to eight pages in one go
- up to 32 stored Teletext pages
- function extended by automatic language-dependent character selection
- switchover facility PAL/NTSC/D2-MAC
- ghost row (26) access for use of extended character sets e.g. Spain, Czechoslovakia
- full support of FLOF or TOP features

As external RAM can be used either one 64 K × 1 bit Dynamic RAM or one 16 K × 1 bit Dynamic RAM. So, the RAM capacity is flexible to store 8 or 2 pages. The RAMs can be standard types. Via the IM bus the CCU can read from and write into all RAM locations and controls the TPU by loading the appropriate registers in the RAM, so that the TPU can be used to display text from other sources. The TPU can display a list of contents of the stored eight pages (menu) all by itself.

## **Multistandard Teletext Processor for Level 1.5 Teletext with Enhanced Display Capabilities** (44-Pin PLCC Package)

This new multistandard teletext processor in CMOS technology with enhanced display capabilities is specified to handle Level 1.5 Teletext and fits into the DIGIT2000 digital TV system.

All existing teletext standards even more exotic ones like NABTS, ANTIOPE or Closed Caption are supported.

Up to 80 10 × 12-characters per row can be displayed and even RGB pixelwise definition of pictures are possible.

The following features apply for the TPU2740:
- multistandard data access: MAC-VBI and packet data
- magazine and page selection by an 80 MIPS RISC processor
- vertical scrolling function
- full ghost row access
- FLOF/TOP
- flickerfree display optional (100 Hz vertical)
- DRAM interface for one external DRAM of either 256 Kbit, 1 Mbit or 4 Mbit
- storage of: max. 14 pages (512 Kbit DRAM);
  max. 46 pages (1 Mbit DRAM);
  max. 238 pages (4 Mbit DRAM)
- switchover facility PAL, NTSC, SECAM, D2-MAC, D-MAC Packets
- user-definable characters
- full-channel Teletext
- 1 MHz IM bus interface for communication with the CCU
- CCU access to TPU DRAM via IM bus
- input is the digitized video signal (7 bits), supplied in the Gray code by the video Codecs
- ghost compensation eliminates the influence of reflections
- enhanced character resolution (matrix 10 × 12)

**Videotex and Teletext Processor** (68-Pin PLCC Package)

The BVT2710 is specified to handle UK-Teletext (WST World System Teletext) level 1–3 and Videotext (Viewdata) according to the CEPT standard. The display controller part provides an 8 bit wide parallel interface and is capable of every display-function which is prescribed by the CEPT standard. Furthermore some useful additional features have been added. In general this is a display controller with additional teletext-slicer capabilities.

Different to other approaches the system is essentially bitmapped. The display memory is pixel oriented with additional character attributes. It can be used for any display application which makes use of the character attributes prescribed in the CEPT norm but is not restricted in terms of number of different attributes.

The BVT2710 is a N-channel VLSI MOS circuit and contains on a single silicon chip the following functions:

- teletext reception and display (WST)
- FLOF teletext (level 1.5)
- switchover facility PAL/NTSC World System Teletext
- ghost compensation to eliminate the effects of ghost pictures due to reflections
- full channel teletext
- hardware magazine and page selection
- storage of more than 450 pages
- videotex display controller (CEPT norm)
- vertical scrolling
- overlay of a second page in additional window
- horizontal phase comparator
- 50 – 75 Hz vertical frequency for display with parallel decoding of teletext (50 Hz receive, 75 Hz display)
- RGB output (4 Bit D/A-converter)
- DRAM interface
- microcontroller interface (Intel 8051 compatible)

**1024-Bit EEPROM** (14-Pin Plastic Package TO-116)
**4096-Bit EEPROM** (8-Pin Plastic Package)

Electrically erasable programmable read only memories (EEPROM) in N-channel floating-gate technology with the following capacity:

MDA2062:128 words, 8 bits each
NVM3060:512 words, 8 bits each.

These EEPROMs are intended for use as reprogrammable non-volatile memories in conjunction with the CCU2030/2050/2070 series Central Control Units of the DIGIT2000 Digital TV System, or the SAA1293A Remote-Control and Tuning IC. They serve for storing the tuning information, as well as several analog settings, furthermore, alignment information given in the factory when producing the TV set. The stored information remains stored even with the supply voltages switched off. Reading and programming operations are executed via the IM bus.

Input and output signals are TTL level. An address option input provides the possibility to operate two memories in parallel, to obtain a total storage capacity of 2048 bits (two MDA2062) or 8192 bits (two NVM3060).

The programming matrix contains a protectable portion. This part of the memory can only be programmed if the Safe Input $\overline{S}$ is at a high potential. In that way, this portion of the memory is protected against inadvertent reprogramming even if such false informations were received via the IM bus.

In contrary to the MDA2062 the NVM3060 needs only one supply voltage of 5 V because this device contains a charge pump for high programming voltage generation. Additionally a clock oscillator is on-chip.

**Infrared Remote-Control Transmitter IC** (24-Pin Plastic Package)

This integrated CMOS circuit has been developed for infrared remote control of color TV receivers, but can also be used for other applications with advantage. It consumes a minimal current and, due to its large instruction repertoire, is highly flexible in application. Up to 1024 commands can be transmitted by one SAA1250. As receivers either the CCU2030/CCU2050/CCU2070/CCU3000 series Central Control Units for the DIGIT2000 Digital TV System or the SAA1293A Remote-Control and Tuning IC for TV receivers are intended.

Pulsecode-modulated infrared light serves for the transmission of remote-control commands. The information is defined by the varying time intervals between a sequence of very short infrared pulses. This enables the emitter diode to be driven with a high current (1 A or more), thus achieving a large transmission distance and high interference immunity. At the receiver end, a photo-diode converts the IR-transmissions into electrical signals which are amplified in the TBA2800 Infrared Preamplifier IC and fed to the receiver IC, where the signals are converted into the respective commands, e.g. for switching on/off, station selection, for the setting of analog values such as volume, brightness etc., for the control of Teletext, and more.

Each remote-control word contains ten information bits. The transmitter IC SAA1250, therefore, is capable of delivering 1024 different signals. The word is usually structured into four bits and six bits offering 16 addresses and 64 commands.

## **Infrared Remote-Control Transmitter ICs** (24-Pin Plastic Package)

The IRT1250 is a further development based on the well-known SAA 1250. The main differences are the address selection code and the higher output current. The IRT1250 is a CMOS circuit intended for infrared remote control of color TV receivers, but can also be easily used in other applications. It consumes a minimal current and, due to its large instruction repertoire, is highly flexible in application. Up to 512 commands can be transmitted by one IRT1250 transmitter IC. Either the CCU2030/CCU2050/CCU2070/CCU3000 series Central Control Units for the DIGIT2000 Digital TV System or the SAA1293A Remote-Control and Tuning IC can be used to receive the infrared commands.

Pulsecode-modulated infrared light serves for the transmission of remote-control commands. The information is defined by the varying time intervals between a sequence of very short infrared pulses. This enables the emitter diode to be driven with a high current (1 A or more), thus achieving a large transmission distance and high interference immunity.

At the receiver end, a photo-diode converts the IR-transmissions into electrical signals which are amplified in the TBA2800 Infrared Preamplifier IC and fed to the receiver IC where the signals are converted into the respective commands, e. g. for on/off switching, choice of the station to be received, for the setting of analog control values such as volume, brightness etc., for the control of Teletext, and so on. The IRT1260 is identical to the IRT1250 except for the supply voltage which is 3 V only.

## **Infrared Preamplifier IC** (14-Pin Plastic Package TO-116)

Bipolar integrated circuit intended as a receiver preamplifier for the CCU20.. or the infrared remote-control systems designed with the SAA1293A integrated circuit.

The TBA2800 preamplifier IC contains four main parts: gain-controlled amplifier I, amplifier II, pulse-separating amplifier III, and inverter IV. Amplifier I has a wide dynamic range and thus ensures interference-free operation, even at bright ambient light or at intensive infrared light as it comes from infrared sound transmissions or at bright 50-Hz modulated light as it originates from fluorescent lamps. It is also possible for the remote-control transmitter to be near the receiver without causing malfunctions by overdriving the receiver.

Amplifier II further amplifies the signal, and amplifier III separates the pulse-shaped intelligence signal from noise and other unwanted parts. The additional inverter IV inverts the negative output pulses at pin 7 and thus delivers positive output pulses at pin 8. If an additional resistor is inserted between pin 6 and GND, noise immunity is increased. But this is accompanied by a decrease in sensitivity.

## **D/A and Bus Converter IC for IM Bus** (18-Pin Plastic Package)

The MEA2050 D/A and bus converter is an N-channel MOS circuit which converts the digital information on, for example, volume, brightness, contrast and color saturation supplied by the CCU or similar circuits, into analog signals for controlling analog stages.

The MEA2050 receives its input information via the IM bus from the CCU in the form of 16-bit words containing the infrared address in the upper byte and the infrared command in the lower byte.

The supply voltage is 5 V and the current consumption 25 mA max. All outputs have open-drain configuration, the voltage rating being 12 V. At a 4 MHz clock frequency, the analog outputs DA1 to DA8 supply a rectangular 63.5 kHz output signal. This signal contains the information in the pulse/interval ratio which is variable in 64 steps between zero and infinite.

## **Tuner Interface IC** (16-Pin Plastic Package)

Integrated bipolar circuit which converts the band switching and the tuning information delivered in digital form by the CCU20.. or similar PLL circuits into signals suitable for biasing the tuner and band switching diodes of TV tuners. For converting the tuning signals, the MEA2901 contains a D/A converter and an active filter. Input signal for this part of the MEA2901 tuner interface are TTL compatible pulses supplied by the phase comparator of the PLL contained in the CCU20.. For band switching, the MEA2901 contains a decoder binary/one out of four. It is thus possible to transmit the information for the four bands via only two wires from the CCU to the MEA2901. In addition, the MEA2901 has four power switches that supply the current required by the tuner's bandswitch diodes.

## **Remote-Control and Tuning Microcomputer for TV Receivers** (40-Pin Plastic Package or 44-Pin PLCC Package)

The SAA1293A is a microcomputer in N-channel MOS technology. On one silicon chip, it contains all the operating and tuning functions of a modern TV receiver. Thus, along with the MDA2062 or NVM3060 non-volatile memories, the SAA1250, IRT1250 or IRT1260 remote-control transmitter and the TBA2800 preamplifier this offers a very economic solution for TV receivers with a low or average degree of operating comfort in which station selection is by voltage synthesis. Features of the SAA1293A are:

- tuning voltage generation with rate multiplier allows the use of low-cost tuner and avoids problems with different channel tables
- four analog outputs for volume, brightness etc.
- storage of up to 55 stations
- flexible processing due to options set by the equipment manufacturer. Thus a large product range of TV receivers can have the same SAA1293A control microcomputer
- direct interfacing with ITT multipage Teletext system (or SAA5000 family for Teletext) without extra controler for Teletext
- remote control of all functions, including tuning and Teletext
- full two-digit station display
- keyboard with up to 32 keys for direct operation
- various intelligent tuning methods allow free selection of the station location during tuning
- standby mode with automatic mains-on when a station is selected
- multi-standard switch
- output switches for special audio-video modes
- flexible logic for fading in and out of sound and picture while a station is being changed
- bandswitch outputs for four bands
- band indication on the display, no separate indication needed
- fine or normal tuning at four speeds using the remote control
- "service" mode for easy setting up and servicing

## **Audio Conversion and Demodulation Processor** (44-Pin PLCC Package)

This device is a CMOS processor designed to be used in car radio systems, in conjunction with the UDPC1000 Digital Signal Processor. The main tasks of the ACDP1100 are A/D conversion of the analog audio signals before processing in the UDPC1000, source selection, D/A conversion, FM-demodulation, stereo decoding and extraction of ARI signals. Apart from the A/D and D/A converters themselves, the ACDP1100 also contains a considerable number of digital filters necessary in this conjunction, the SIF serial interface for communication with one or two UDPC1000 Digital Signal Processors and the IM bus interface for communication with the controlling microprocessor. There are three main operation modes three which the ACDP1100 is intended:

**MPX Mode:** This mode actually means the reception of an FM station, where the FM demodulation must be done in the conventional tuner. The extraction of the ARI signals and pilot tone will be done digitally within the ACDP1100.

**AM/AF Mode:** In this mode the ACDP1100 essentially works transparently. This mode is intended for AM reception with a conventional tuner, or for processing signals originating from analog sources. In the AM/AF mode the MPX input of the ACDP1100 remains active to enable monitoring of the traffic information (ARI) also during playback of a compact disc or a digital cassette.

**XDS Mode:** Digital audio signals supplied by an external digital source (XDS) are processed in this operation mode, e.g. signals from a CD player or a DAT (digital audio tape) recorder. In addition, the input or systems of the ACDP remain active to perform monitoring of the traffic information (ARI) also during playback of a compact disc or a digital cassette.

## **Digital Signal Processor** (44-Pin PLCC Package)

The UDPC1000 Digital Signal Processor was designed in Si-gate CMOS technology and has been developed for fast signal processing in commercial applications.

The central processing unit (CPU) comprises a 16 × 10 bit multiplier with adder. The basic operations of the CPU are multiplication and addition or multiplication and subtraction. They last less than 120 ns and can be executed continuously one after the other in one processing sequence to achieve maximum throughput. For this purpose the preparatory operations can be executed in parallel using the „pipelining" technique.

The standard configuration of a system containing the UDPC1000 comprises A/D conversion, digital signal processing in the UDPC 1000, D/A conversion, and control by a microcomputer. For application in a car radio, A/D as well as D/A conversion including source selection can be done by the ACDP1100 Audio Conversion and Demodulation Processor which was developed especially for this task. As a controller, a standard microprocessor may be used according to the system's requirements.

**Features**

- instruction cycle 60 ns minimum
- fixed-point, two's complement arithmetic
- 16 × 10 → 20 bit multiplication in 120 ns (incl. add, fetch, move result)
- 20-bit accumulator
- internal memory range: program ROM: 1 K × 15 bit
  data RAM: 160 × 16 bit
  coefficient RAM: 72 × 10 bit
  coefficient ROM: 128 × 10 bit
- multi-function instructions
- triple subroutine stack
- input/output: serial (fast, up to 8.25 Mbit/s)
  serial (slow, IM bus)
- cross assembler in FORTRAN (standard 77 with a few additional functions available on DEC computers)
- emulator IC available with external program memory

## **Tone Dialler Circuit** (16-Pin Plastic Package)

This CMOS circuit uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies which are mixed together to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialling.

### Features

- Minimum external parts count
- High-accuracy tones
- Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip
- Uses inexpensive 3.58 MHz TV color burst crystal
- Invalid key entry can result either single tone or no tone
- Chip disable allows any key down output to function from keyboard input without generating tones.

### Description

The SBA5089 was designed specifically for integrated tone dialler applications that require the following: fixed supply operation, negative true keyboard input, Chip Disable input, stable output tone level, and Any Key Down output that is open circuit when no keyboard buttons are pushed and pulls to the $V_B$ supply when a button is pushed. Keyboard entries to the SBA5089 cause the selection of the proper divider ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.
D to A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sinewave and requires little filtering for low distortion applications. The same operational amplifier that accomplishes the current to voltage transformation necessary for the D to A converter also mixes the low and high group signals. Frequency stability of this type of tone generation is such that no frequency adjustment is needed to meet standard DTMF specifications.

## **Tone Ringer IC** (14-Pin Plastic Package TO-116)

This integrated CMOS circuit replaces the customary electromechanical telephone ringer and calls the subscriber by a melodic tone sequence, using a small magnetic or piezoceramic sound transducer. The tone ringer circuit, together with its transducer is powered by the ringing current from the exchange. This makes it compatible with the conventional telephone network and, furthermore, no battery or mains connections are needed.

### Functional Description

The tone ringer circuit normally derives the power required for its operation from the ringing AC supplied by the exchange via lines a and b.

Together with the loop resistance, the 1 μF isolating capacitor and a 2.2 kΩ resistor, the ringing generator in the exchange operates as an alternating-current source. The 2.2 kΩ resistor is needed to ensure a minimum impedance. The supplied alternating current is fed to pins 5 and 7 of the SAA1094-2 and is rectified by means of an integrated bridge circuit in the SAA1094-2. The rectified current charges the electrolytic capacitor at pins 4 and 6. The direct voltage produced across this capacitor mainly depends on the loop resistance and on the ringing frequency and is limited to the operating voltage $V_Z$ of the Zener diode integrated in the SAA1094-2. Tone ringing is switched on when the DC voltage across $C_1$ has reached the value of about 6 V. The switch-off threshold at decreasing supply voltage is about 3 V.

## **Telephone Subset Amplifier** (18-Pin Plastic Package)

### Features

- Automatic compensation of line losses by using a gain-controlled amplifier
- Very accurate (±2 dB) send, receive and VF (voice frequency) gains to achieve optimum system performance
- Low supply current obtained entirely from a small proportion of the line current
- Cancellation circuit to achieve required reduction in sidetone
- Balanced microphone input circuit for reduced sidetone
- Operation can be achieved if the subsets are paralleled
- Stabilised D.C. output for powering external VF oscillator
- Send, VF and receive gains can be preset externally by choice of resistors
- Both low and high frequency characteristics (usually roll off's) of the send gain can be separately adjusted by external capacitors
- Control of quiescent operating point on curve relating D.C. line current with amplifier gain
- Low send and receive noise
- Mute facility for send and receive amplifiers during dialling

### Description

The TEA1045 is a bipolar integrated circuit specially designed for use in a telephone subset to amplify the output from the handset microphone to the telephone line and to amplify the incoming speech on the line to the earpiece transducer. The microphone and earpiece transducers can be of the same type and construction.
The overall characteristics of the TEA1045 are very well defined and controlled. Both send and receive gains within the integrated circuit have only a small overall spread of 4 dB (±26% about nominal). With line impedance and set-gain resistors closely controlled the performance of the subset is well defined in the system.

## **Silicon Click Suppressor** (DO-35 Package)

Monolithic integrated analog circuit with symmetric V/I-characteristic for use as voltage limiter, e.g. as click suppressor in telephone subsets.

| Type | Maximum Ratings | | | | Characteristics at $T_A = 25$ °C | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Operating Current at $T_A = 25$ °C | Surge Current at t = 100 μs | Power Dissipation at $T_A = 25$ °C | Junction Temperature | Forward Voltage Drop at $\|I_F\|$ = 100 mA | Dynamic Resistance at $\|I_F\|$ = 2 mA, f = 1 kHz | Residual Attenuation at $R_G = R_L = 600\ \Omega$, f = 0.2...4 kHz Voltage Level at the Generator | | |
| | | | | | | | −4 N | −0,5 N | 0 N |
| | ± $I_F$ mA | ± $I_{FSM}$ A | $P_{tot}$ mW | $T_j$ °C | $\|V_F\|$ V | $r_F$ Ω | D N | D N | D N |
| | 150 | 1 | 300 | 150 | <1.35 | 20 (<29) | <0.05 | 0.05 | 1.8 (>0.5) |

### **Car Clock IC with Digital Adjustment, 0.5 Hz Output and Additional 64 Hz Signal** (16-Pin Plastic Package)

CMOS circuit for crystal-controlled analog car clocks with 12 V (6... 16.5 V) supply voltage having an additional 64 Hz push-pull output supplying a time base signal e. g. for recording speedometers. The SAF0300 consists of an oscillator circuit, a fixed 4 : 1 frequency divider, an adjustable frequency divider which is variable in 127 steps and covering the range from $2^{14}$ : 1 to ($2^{14} + 2^2$) : 1, a motor driver stage in bridge configuration and the 64 Hz push-pull output.

Apart from the crystal the oscillator does not require any additional components. The correct output frequency may be set by seven adjustment terminals with an accuracy of $10^{-6}$. At 4.194 812 MHz oscillator frequency the bridge output (pins 12/13) supplies a squarewave signal of 0.5 s pulse duration and 0.5 Hz frequency if the adjustable frequency divider is set to the center position. Every second a current pulse of alternate direction flows in the motor coil. Output 1 (pin 1) supplies the additional 64 Hz squarewave signal with a pulse duty factor of 0.5.

The adjustable frequency divider has been designed so that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 16. If one or more adjustment terminals are grounded (taken to pin 14), the output frequency decreases. Pin 8 gives the smallest adjustment step of 1.9 ppm. Pin 7 offers the nextlarger step of 3.8 ppm and so forth, up to pin 2 which enables an adjustment step of 122 ppm to be obtained. If all adjustment terminals are grounded, the output frequency is reduced by 242 ppm.

### **Car Clock IC with Digital Adjustment and 0.5 Hz Output** (14-Pin Plastic Package TO-116)

CMOS circuit for use in crystal-controlled analog car clocks operating on 12 V (6...16,5 V) supply voltage. The SAJ300R contains an oscillator circuit, a fixed 4 : 1 frequency divider, an adjustable frequency divider and a motor driver stage. The adjustable frequency divider of the SAJ300R has an adjustment range from $2^{21}$ : 1 to ($2^{21} + 2^9$) : 1.

Except for the crystal, the oscillator requires no additional components. The trimmer capacitor previously needed for frequency adjustment has been taken over by the variable frequency divider. Seven adjustment pins are provided. They are used to set the divider ratio to the required value with an accuracy of $10^{-6}$. With an oscillator frequency of 4.194 812 MHz the series-connected push-pull output stage supplies a symmetrical squarewave signal with a pulse duty factor of 0.5. The frequency of this output signal is 0.5 Hz if the variable frequency divider is set to the center. Due to the differentiating effect of the motor capacitors pulses of alternate direction occur in the motor coil.

The adjustable frequency divider has been designed so that the maximum output frequency is set when all adjustment pins are either open circuit or connected to pin 14. If one or more adjustment pins are grounded (taken to pin 13) the output frequency decreases. Pin 7 gives the smallest adjustment of 1.9 ppm. Pin 6 affords the nextlarger step of 3.8 ppm and so forth, up to pin 1 which enables an adjustment step of 122 ppm to be obtained.

### **CMOS Car Clock IC with Electrical Forward Setting** (16-Pin Plastic Package)

The CLK5010 is designed for driving analog clocks that advance at either second or minute intervals. With minute-controlled mechanisms, forward setting is done electrically by pressing a pushbutton switch. With second-controlled mechanisms, the minute and second hands must be set mechanically.

The IC contains an oscillator circuit for a 4.194812 MHz crystal and a switchable frequency divider whose output frequency in the normal mode is 0.5 Hz for clocks with a seconds' hand or 1/120 Hz for minute-controlled mechanisms. Change-over takes place at the min/$\overline{\text{sec}}$ input. With seven tuning pins of the frequency divider, the output frequency can be adjusted to 0.5 Hz or 1/120 Hz to an accuracy of $\pm$0.95 ppm. In the normal mode, the conduction phase of the alternating current through the motor winding is 125 ms. The motor makes a step every time the current direction changes.

Electrical forward setting is actuated with a pushbutton switch at the setting input. Each time the button is briefly pressed, a motor step takes place in forward direction. If the button is pressed for more than approx. 1.2 s, fast electrical setting takes place with 21 steps per second. When the button is released, the second counter is reset so that the clock is synchronized to the full minute.

### **CMOS Car Clock IC with Electrical Setting** (16-Pin Plastic Package)

The CLK5011 is designed for driving analog clocks that advance at either second or minute intervals. With minute-controlled mechanisms, settings are done electrically either forward or backward by actuating a change-over switch. With second-controlled mechanisms, the minute and second hands must be set mechanically.

The IC contains an oscillator circuit for a 4.194812 MHz crystal and a switchable frequency divider whose output frequency in the normal forward mode is 0.5 Hz for clocks with a seconds' hand or 1/120 Hz for minute-controlled mechanisms. Change-over takes place at the min/sec input. With six tuning pins of the frequency divider, the output frequency can be adjusted to 0.5 Hz or 1/120 Hz to an accuracy of $\pm$1.90 ppm.

The step motor is operated by a main winding L1 at the motor outputs MO1 and MO2 and an auxiliary winding L2 at the motor outputs MO2 and MO3. L2 is only provided for minute movements and allows the direction of rotation of the step motor to be changed. In the normal mode, the conduction phase of the alternating current through the motor winding(s) is 125 ms. The motor makes a step every time the current direction changes. In the normal mode of a clock with a second movement, the connections MO1 and MO2 are controlled in phase opposition wit the 0.5 Hz frequency.

In the minute mode, MO3 is controlled in the normal mode (with a frequency of 1/120 Hz) and in phase with MO1 for forward setting (L1 and L2 parallel). MO1 and MO3 are controlled in phase opposition (L1 and L2 in series) for backward setting (MO2 disabled).

When the change-over switch is open, the clock is in the normal mode. Each time the switch is briefly actuated (to R or L), a motor step takes place forwards or backwards. If the switch is pressed to R or L for more than approx. 1.2 s, fast electrical setting takes place in the corresponding direction with 21 steps per second. When the switch is released, the second counter is reset so that the clock is synchronized to the full minute.

## **Multitimer IC** (18-Pin Plastic Package)

This IC is designed for use in motor vehicles. It contains:
- the windscreen wiper pulse generator
- the turn signal flasher
- the control circuit for a full-facility rear heating system

Wiper pulse generator:
In normal wiping mode the post wiping time after switching off is 4 s. The post wiping time is retriggerable. In the intermittent operation mode the pulse length is 0.6 s, the interval time 5 s. A start command for normal wiping has priority over a command for intermittent operation. The latter is resumed when the post wiping time has elapsed, starting from a no-pulse period.

Turn signal flasher:
The turn signal flasher starts with the bright phase. 90 pulses/min. are delivered with a 50% duty cycle at the flasher output. The flashing frequency is doubled due to lamp failure. When the flasher is used in the hazard warning mode the duty cycle (bright phase) is reduced to 35% in order to spare the battery.

Rear screen heating:
After switching on, the rear screen heating system is switched off automatically after 15 min. The function is indicated by a lamp. If the battery reaches a specified undervoltage value, heating of the rear screen is interrupted. When this happens, the indictor lamp flashes at 1.5 Hz. The interruption of the heating is terminated, when the battery voltage reaches a sufficient value again. The rear screen heating system is not retriggerable.

## **Speedometer and Mileage Indicator IC** (18-Pin Plastic Package with 2 Cooling Fins)

The UAF1025 is a bipolar integrated circuit designed for speedometers and mileage indicators in automobiles. It comprises a monostable flip-flop with Schmitt trigger input which is controlled either by a reed contact or a proximity switch (dropout oscillator) placed, for example, at the drive shaft of the gearbox and which supplies one rectangular pulse per shaft rotation. The rate of these pulses is proportional to the car's speed, and the pulses control a pulsed current source (meter driver), a frequency divider and a pulse amplifier as shown in the block diagram.

The speed-dependent output current of the meter driver is indicated by a moving-coil meter giving the car's speed. The frequency divider, whose division ratio can be selected by means of pin 11 to be $2^5$, $2^6$ or $2^7$, supplies pulses for controlling a stepping motor which drives the mileage counter. The pulses from the monostable are also amplified and output via pin 3 to control a taximeter or a tachograph.

To protect the UAF1025 against high-voltage peaks from the car supply system, an external filtering RC element is required. The supply current for the stepping motor does not flow through this network thereby ensuring reliable drive for the mileage counter even at low battery voltage. Two limiting diodes connected to the filtered supply protect the stepping motor buffer against overvoltage peaks and a third limiting diode protects the taximeter output pin 3.

## **Speedometer and Mileage Indicator IC Kit** (18-Pin Plastic Package)

This IC kit is intended for designing a programmable speedometer and mileage indicator for cars with 12 V or 24 V supplies. Due to its programmability, for which seven programming pins are provided, the circuit can be easily adapted to different cars and different tyre diameters. An additional pulse output is provided for driving, e.g., a taximeter.

**SAF1091** – proximity switch, voltage regulator, overvoltage protection (bipolar technology)

This IC detects the car's speed by means of an LC oscillator whose coil is placed near the drive shaft of the gearbox and is influenced by a piece of metal attached to this shaft. Each rotation causes a dropout in oscillation, in this way producing a pulse train whose frequency is equal to the rotation speed of the shaft and thus proportional to the speed of the vehicle. The pulses are fed to the SAF1092 Logic IC for processing. After this, they are fed back to the SAF1091 where they control a current source for indicating the speed on a moving-coil meter and a stepping motor for registering the miles covered.

**SAF1092** – logic IC and frequency divider (CMOS technology)

The main part of this IC is a programmable counter which counts the periods of a 470 kHz (or 50 kHz) oscillator, controlled by the input pulses from the SAF1091, and a divider which can be set to $2^{13}$ or $2^{14}$ as required. This divider, via the SAF1091, drives the two coils of the stepping motor for mileage indication.

**Pulse Shaper for Rev-Counters** (8-Pin Plastic Package)

The monolithic integrated circuit SAK215 is designed for use in revolution counters of cars and for other applications like frequency to current converters. By use of suitable external circuitry the revolution counter can be adapted to engines with two to eight cylinders. It is designed for a nominal 12 V DC supply.

The Figure shows the operating circuit of a revolution counter with FSD = 6000 RPM (two ignition pulses per turn of the crank-shaft) at a nominal battery voltage of 12 V. Current consumption of the IC is about 12 mA.

**10 V Car Voltage Regulator** (Plastic Package TO-202/1)

Monolithic integrated voltage regulator in bipolar technology, especially designed for stabilized power supplies of car instrumentation in cars with 12 V accumulators. This IC features narrow tolerance on output voltage, a low temperature coefficient and is equipped with an automatic current limiter and a thermal overload protection which prevents destruction of the IC in case of accidental overloads, for example short-circuits.

A sufficiently large cooling fin must be provided, to ensure that under normal working conditions the max. permissible junction temperature is not exceeded, and the thermal overload protection does not operate.

## **LCD Display Driver** (52-Pin Dil Plastic SMD Package)

This VLSI circuit in CMOS technology is intended for driving a liquid-crystal display. Optionally, static or dynamic (two-fold multiplex) display modes can be selected. In static operation, four digits of eight segments each can be driven. In dynamic multiplex operation, this number is doubled to eight digits. The SAF1079 LCD Display Driver can also be cascaded, one IC being the master which supplies the backplane signals, with up to seven slaves, so that eight times eight giving sixty-four digits can be driven by eight SAF1079 ICs.

The information on the segments to be displayed is fed to the ICs via a Data and a Clock line. The sequence of the segments displayed is given by the sequence of the valid Data, i.e. the first Data bit controls segment 0, the 64$^{th}$ bit segment 63. Output BP1 is used as the backplane signal for Data bits 0 to 31, and BP2 for bits 32 to 63.

The master IC processes the DI (Data Input), SCLI (Shift Clock Input) and BCLI (Backplane Clock Input) signals. Data and shift clock are supplied for driving the slaves, by the DO and SCLO outputs. The BCLI backplane clock is divided by 128 internally and is available at the Sync 1 output for cascading. Three address inputs A0 to A2 are provided for deciding which of the cascaded drivers receives the information supplied by the Data line. Static or dynamic operation is selected by the $V_{XNS}$ input.

## **High-Speed A/D-D/A-Converters** (40-Pin Plastic Package)

VLSI circuits in CI technology, featuring the following circuits:
- a high-speed flash type 8-bit A/D converter
- a high-speed low-glitch 10-bit D/A converter, designed as an R-2R network with switched current sources
- various auxiliary circuits, as reference voltage sources, preamplifier, input clamping circuit, and feed-in output amplifier.

UVC3130 has been developed for use in all applications which call for a high-speed A/D-D/A converter. It can be used to decode television signals in Pay-TV converters or for D2-MAC converters used in direct satellite broadcast. Other applications can be seen in industrial electronics, e.g. in conjunction with digital signal processing. Although UVC3130 was initially designed as high-speed codec for the video range, it can be used with equal benefits for lower frequencies, even down to zero.

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. An impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input, in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of that circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected. Further, the input is equipped with switches which optionally provide operation with keyed clamping or peak clamping or without clamping. Also the D/A converter's reference voltage is generated on-chip, and a gated amplifier is arranged at the output of the D/A converter so that an external analog signal can be fed-in instead of the signal delivered by the D/A converter.

Separate clock inputs are provided for the A/D converter and the D/A converter thus enabling the application of time compression procedures. All inputs and outputs are TTL compatible.

**UVC3120** is generally identical to the UVC3130, except that the input amplifier, voltage reference and clamping circuitry of the A/D section have been omitted.

To meet different application requirements these converters are classified into for groups with respect to the linearity of the D/A converter:

| Marking | Linearity D/A |
|---|---|
| UVC3130-10; UVC3120-10 | 10 Bit |
| UVC3130-09; UVC3120-09 | 9 Bit |
| UVC3130-08; UVC3120-08 | 8 Bit |
| UVC3130-07; UVC3120-07 | 7 Bit |

## **Temperature-Compensated Zener Diodes** (DO-35 Package)

Linear integrated circuits generating an extremely constant temperature-compensated reference voltage with an extremely short thermal run-in time, particularly suitable for stabilizing the tuning voltage of electronic tuned TV and radio receivers employing capacitance diodes.

| Type | Operating Voltage at $I_Z$ = 5 mA* | | Dynamic Resistance at $I_Z$ = 5 mA | | Temperature Coefficient of Op. Voltage at $I_Z$ = 5 mA | | | Thermal Run-in Time | Operating Current at $T_A$ = 45 °C | Junction Temperature |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | x $10^{-5}$/°C | | | | | |
| | min. V | max. V | typ. Ω | max. Ω | min. | typ. | max. | seconds | max. mA | max. °C |
| | 6.4 | 7.1 | 12 | 25 | −10 | −2 | +5 | 20 | 36 | 150 |
| | 8 | 10 | 10 | 25 | −10 | −2 | +5 | 20 | 27 | 150 |
| | 10 | 12 | 10 | 25 | −10 | −2 | +5 | 20 | 19 | 150 |
| | 16 | 20 | 11 | 25 | −10 | −2 | +5 | 20 | 13 | 150 |
| | 20 | 24 | 11 | 25 | −10 | −2 | +5 | 20 | 10 | 150 |
| | 24 | 30 | 12 | 25 | −10 | −2 | +5 | 20 | 8 | 150 |
| | 30 | 32 | 12 | 25 | −10 | −2 | +5 | 20 | 7 | 150 |
| | 32 | 34 | 12 | 25 | −10 | −2 | +5 | 20 | 7 | 150 |
| | 34 | 36 | 12 | 25 | −10 | −2 | +5 | 20 | 7 | 150 |

*Measured with pulses tp = 20 ms

## **Silicon Stabilizer Diodes** (DO-35 Package) and **LL1,5 to LL5,1 Silicon Stabilizer Diodes** (MiniMELF Package)

The end of the device marked with the cathode ring is to be connected:

ZTE/LL1,5 and ZTE/LL2 to the negative pole of the supply voltage
ZTE/LL2,4...ZTE/LL5,1 to the positive pole of the supply voltage

| Type | Stabilized Voltage at $I_Z$= 5 mA* | | Dynamic Resistance at $I_Z$= 5 mA f = 1 kHz | | Temperature Coefficient of Stab. Volt. at $I_Z$ = 5 mA | max. Thermal Resistance | Operating Current at $T_A$ = 25 °C | Forward Current at $T_A$ = 25 °C | Power Dissipation at $T_A$ = 25 °C | Junction Temperature |
|---|---|---|---|---|---|---|---|---|---|---|
| | min. V | max. V | typ. Ω | max. Ω | $10^{-4}$/°C | °C/mW | max. mA | max. mA | max. mW | max. °C |
| | 1.35 | 1.55 | 13 | 20 | −26 | 0.4 | 120 | 100 | 300 | 150 |
| | 2.0 | 2.3 | 18 | 30 | −26 | 0.4 | 120 | 100 | 300 | 150 |
| | 2.2 | 2.56 | 14 | 20 | −34 | 0.4 | 120 | 100 | 300 | 150 |
| | 2.5 | 2.9 | 15 | 20 | −34 | 0.4 | 105 | 100 | 300 | 150 |
| | 2.8 | 3.2 | 15 | 20 | −34 | 0.4 | 95 | 100 | 300 | 150 |
| | 3.1 | 3.5 | 16 | 20 | −34 | 0.4 | 90 | 100 | 300 | 150 |
| | 3.4 | 3.8 | 16 | 25 | −34 | 0.4 | 80 | 100 | 300 | 150 |
| | 3.7 | 4.1 | 17 | 25 | −34 | 0.4 | 75 | 100 | 300 | 150 |
| | 4.0 | 4.6 | 17 | 25 | −34 | 0.4 | 65 | 100 | 300 | 150 |
| | 4.4 | 5.0 | 18 | 25 | −34 | 0.4 | 60 | 100 | 300 | 150 |
| | 4.8 | 5.4 | 18 | 25 | −34 | 0.4 | 55 | 100 | 300 | 150 |

*Measured with pulses tp = 20 ms

with plastic package 10D3 according to DIN 41870 (≈TO-92). On special request, these transistors will also be produced with TO-18 pin configuration.

| Type | Pin Config. | $V_{CEO}$ | $h_{FE}$ | at $V_{CE}/I_C$ | $V_{CEsat}$ | at $I_C/I_B$ | $I_{CES}$ | at $V_{CE}$ | $f_T$ | at $V_{CE}/I_C$ | $C_{ob}$ | at $V_{CB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | | V/mA | max. V | mA/mA | max. nA | V | MHz | V/mA | max. pF | V |
| | B | 20 | 35–100 | 1/1 | 0.4 | 30/3 | 100[3] | 15 | 150 | 5/10 | typ. 4.0 | 10 |
| | B | 20 | 80–250 | 1/1 | 0.4 | 30/3 | 100[3] | 15 | 150 | 5/10 | typ. 4.0 | 10 |
| | B | 20 | 200–600 | 1/1 | 0.4 | 30/3 | 100[3] | 15 | 150 | 5/10 | typ. 4.0 | 10 |
| | B | 45 | 100–630 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 45 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 45 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 45 | 250–630 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 100–630 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 250–630 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 30 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 30 | 250 | 5/10 | typ. 2.5 | 10 |
| | B | 30 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 30 | 250 | 5/10 | typ. 2.5 | 10 |
| | B | 45 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 50 | 250 | 5/10 | typ. 2.5 | 10 |
| | B | 45 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 50 | 250 | 5/10 | typ. 2.5 | 10 |
| | B | 60 | 50–460 | 5/2 | 0.25 | 100/10 | 100[3] | 30 | 200 | 5/50 | typ. 3 | 10 |
| | B | 80 | 50–460 | 5/2 | 0.25 | 100/10 | 100[3] | 40 | 200 | 5/50 | typ. 3 | 10 |
| | B | 100 | 50–460 | 5/2 | 0.25 | 100/10 | 100[3] | 60 | 200 | 5/50 | typ. 3 | 10 |
| | B | 60 | 120–220 | 5/2 | 0.25 | 100/10 | 100[3] | 30 | 200 | 5/50 | typ. 3 | 10 |
| | B | 60 | 180–460 | 5/2 | 0.25 | 100/10 | 100[3] | 30 | 200 | 5/50 | typ. 3 | 10 |
| | B | 80 | 120–220 | 5/2 | 0.25 | 100/10 | 100[3] | 40 | 200 | 5/50 | typ. 3 | 10 |
| | B | 80 | 180–460 | 5/2 | 0.25 | 100/10 | 100[3] | 40 | 200 | 5/50 | typ. 3 | 10 |
| | B | 100 | 120–220 | 5/2 | 0.25 | 100/10 | 100[3] | 60 | 200 | 5/50 | typ. 3 | 10 |
| | B | 65 | 110–220 | 5/2 | 0.6 | 100/5 | 15 | 80 | 300 | 5/10 | 6.0 | 10 |
| | B | 65 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 80 | 300 | 5/10 | 6.0 | 10 |
| | B | 45 | 110–220 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6.0 | 10 |
| | B | 45 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6.0 | 10 |
| | B | 45 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6.0 | 10 |
| | B | 30 | 110–220 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6.0 | 10 |
| | B | 30 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6.0 | 10 |
| | B | 30 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6.0 | 10 |
| | B | 30 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6.0 | 10 |
| | B | 30 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6.0 | 10 |
| | B | 45 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6.0 | 10 |
| | B | 45 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6.0 | 10 |
| | E | 40 | 50–150 | 1/10 | 0.3 | 50/5 | 50[4] | 30 | min. 250 | 20/10 | 4 | 5 |
| | E | 40 | 100–300 | 1/10 | 0.3 | 50/5 | 50[4] | 30 | min. 300 | 20/10 | 4 | 5 |
| | E | 25 | 120–360 | 1/2 | 0.3 | 50/5 | 50[3] | 20 | min. 300 | 20/10 | 4 | 5 |
| | E | 40 | 50–150 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 200 | 10/20 | 6.5 | 5 |
| | E | 40 | 100–300 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 250 | 10/20 | 6.5 | 5 |
| | E | 30 | 100–300 | 10/150 | 1.6 | 500/50 | 10[3] | 50 | min. 250 | 20/20 | 8.0 | 10 |
| | E | 40 | 100–300 | 10/150 | 1.0 | 500/50 | 10[3] | 60 | min. 300 | 20/20 | 8.0 | 10 |

[1]) Low Noise Type
[2]) Extremely Low Noise Type
[3]) $I_{CBO}$
[4]) $I_{CEV}$ at $V_{EB}$ = 3 V
[5]) $I_{CEV}$ at $V_{EB}$ = 0.4 V

(Plastic Package TO-236)

| Type | Marking Code | $V_{CEO}$ | $h_{FE}$ | at $V_{CE}/I_C$ | $V_{CEsat}$ | at $I_C/I_B$ | $I_{CES}$ | at $V_{CE}$ | $f_T$ | at $V_{CE}/I_C$ | $C_{ob}$ | at $V_{CB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | | V/mA | max. V | mA/mA | max. nA | V | MHz | V/mA | max. pF | V |
| | 6A | 45 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | 12 | 10 |
| | 6B | 45 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | 12 | 10 |
| | 6C | 45 | 250–600 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | 12 | 10 |
| | 6E | 25 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | 12 | 10 |
| | 6F | 25 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | 12 | 10 |
| | 6G | 25 | 250–600 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | 12 | 10 |
| | 1A | 65 | 110–220 | 5/2 | 0.6 | 100/5 | 15 | 80 | 300 | 5/10 | 6 | 10 |
| | 1B | 65 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 80 | 300 | 5/10 | 6 | 10 |
| | 1E | 45 | 110–220 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6 | 10 |
| | 1F | 45 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6 | 10 |
| | 1G | 45 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6 | 10 |
| | 1J | 30 | 110–220 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6 | 10 |
| | 1K | 30 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6 | 10 |
| | 1L | 30 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6 | 10 |
| | 2B | 30 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6 | 10 |
| | 2C | 30 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 30 | 300 | 5/10 | 6 | 10 |
| | 2F | 45 | 200–450 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6 | 10 |
| | 2G | 45 | 420–800 | 5/2 | 0.6 | 100/5 | 15 | 50 | 300 | 5/10 | 6 | 10 |
| | AA | 32 | 120–220 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 250 | 5/10 | 4.5 | 10 |
| | AB | 32 | 180–310 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 250 | 5/10 | 4.5 | 10 |
| | AC | 32 | 250–460 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 250 | 5/10 | 4.5 | 10 |
| | AD | 32 | 380–630 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 250 | 5/10 | 4.5 | 10 |
| | AG | 45 | 120–220 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 250 | 5/10 | 4.5 | 10 |
| | AH | 45 | 180–310 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 250 | 5/10 | 4.5 | 10 |
| | AJ | 45 | 250–460 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 250 | 5/10 | 4.5 | 10 |
| | AK | 45 | 380–630 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 250 | 5/10 | 4.5 | 10 |
| | 6R | 30 | 100–300 | 10/50 | 1.6 | 500/50 | 10[3] | 50 | min. 250 | 20/20 | 8 | 10 |
| | 6S | 40 | 100–300 | 10/50 | 1.0 | 500/50 | 10[3] | 60 | min. 300 | 20/20 | 8 | 10 |
| | 1M | 40 | 50–150 | 1/10 | 0.3 | 50/5 | 50[4] | 30 | min. 250 | 20/10 | 4 | 5 |
| | 1N | 40 | 100–300 | 1/10 | 0.3 | 50/5 | 50[4] | 30 | min. 300 | 20/10 | 4 | 5 |
| | 1R | 25 | 120–360 | 1/2 | 0.3 | 50/5 | 50[3] | 20 | min. 300 | 20/10 | 4 | 5 |
| | 6T | 40 | 50–150 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 200 | 10/20 | 6.5 | 5 |
| | 6U | 40 | 100–300 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 250 | 10/20 | 6.5 | 5 |

Normally, the transistors BC817, BC818 and BC846 to BC850 have the following pin configuration: 1 = collector, 2 = base, 3 = emitter. They are also available with inverted configuration: 1 = collector, 2 = emitter, 3 = base, this being indicated by the suffix "R" next to the type designation and the marking code. Example: type BC846AR is indicated as 1AR.

The transistors IMBT2222, IMBT2222A, IMBT3903, IMBT3904, IMBT4124, IMBT4400, IMBT4401 have the following pin configuration: 1 = collector, 2 = base, 3 = emitter.

Normally, the transistors BCW60 to BCX70 have the following pin configuration: 1 = collector, 2 = base, 3 = emitter. These types are also available with inverted configuration: 1 = collector, 2 = emitter, 3 = base. The type designation and the marking is the following:

| Type | Marking |
|---|---|
| BCW60RA | AO |
| BCW60RB | AP |
| BCW60RC | AR |
| BCW60RD | AS |
| | |
| BCX70RG | AU |
| BCX70RH | AW |
| BCX70RJ | AX |
| BCX70RK | AY |

[1]) Low Noise Type
[2]) Extremely Low Noise Type
[3]) $I_{CBO}$
[4]) $I_{CEV}$ at $V_{EB}$ = 3 V
[5]) $I_{CEV}$ at $V_{EB}$ = 0.4 V

with plastic package 10D3 according to DIN 41870 (≈TO-92). On special request, these transistors will also be produced with TO-18 pin configuration.

| Type | Pin Config. | $-V_{CEO}$ | $h_{FE}$ | at $-V_{CE}/-I_C$ | $-V_{CEsat}$ at $-I_C/-I_B$ | | $-I_{CES}$ at $-V_{CE}$ | | $f_T$ at $-V_{CE}/-I_C$ | | $C_{ob}$ at $-V_{CB}$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | | V/mA | max. V | mA/mA | max. nA | V | MHz | V/mA | max. pF | V |
| | B | 20 | 35–100 | 1/1 | typ. 0.4 | 30/3 | 100[3] | 15 | 180 | 5/10 | typ. 3.0 | 10 |
| | B | 20 | 80–250 | 1/1 | typ. 0.4 | 30/3 | 100[3] | 15 | 180 | 5/10 | typ. 3.0 | 10 |
| | B | 20 | 200–600 | 1/1 | typ. 0.4 | 30/3 | 100[3] | 15 | 180 | 5/10 | typ. 3.0 | 10 |
| | B | 45 | 100–630 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 45 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 45 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 45 | 250–630 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 100–630 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 25 | 250–630 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | typ. 12 | 10 |
| | B | 30 | min. 40 | 5/0.01 | 0.6 | 100/5 | 15 | 30 | 200 | 5/10 | typ. 4.5 | 10 |
| | B | 30 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 30 | 200 | 5/10 | typ. 4.5 | 10 |
| | B | 30 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 30 | 200 | 5/10 | typ. 4.5 | 10 |
| | B | 45 | min. 40 | 5/0.01 | 0.6 | 100/5 | 15 | 50 | 200 | 5/10 | typ. 4.5 | 10 |
| | B | 45 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 50 | 200 | 5/10 | typ. 4.5 | 10 |
| | B | 45 | min. 100 | 5/0.01 | 0.6 | 100/5 | 15 | 50 | 200 | 5/10 | typ. 4.5 | 10 |
| | B | 60 | 50–460 | 5/2 | 0.25 | 100/10 | 100[3] | 30 | 200 | 5/50 | typ. 3 | 10 |
| | B | 80 | 50–460 | 5/2 | 0.25 | 100/10 | 100[3] | 40 | 200 | 5/50 | typ. 3 | 10 |
| | B | 100 | 50–460 | 5/2 | 0.25 | 100/10 | 100[3] | 60 | 200 | 5/50 | typ. 3 | 10 |
| | B | 60 | 120–220 | 5/2 | 0.25 | 100/10 | 100[3] | 30 | 200 | 5/50 | typ. 3 | 10 |
| | B | 60 | 180–460 | 5/2 | 0.25 | 100/10 | 100[3] | 30 | 200 | 5/50 | typ. 3 | 10 |
| | B | 80 | 120–220 | 5/2 | 0.25 | 100/10 | 100[3] | 40 | 200 | 5/50 | typ. 3 | 10 |
| | B | 80 | 180–460 | 5/2 | 0.25 | 100/10 | 100[3] | 40 | 200 | 5/50 | typ. 3 | 10 |
| | B | 100 | 120–220 | 5/2 | 0.25 | 100/10 | 100[3] | 60 | 200 | 5/50 | typ. 3 | 10 |
| | B | 65 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 80 | 150 | 5/10 | 6.0 | 10 |
| | B | 65 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 80 | 150 | 5/10 | 6.0 | 10 |
| | B | 45 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | B | 45 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | B | 45 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | B | 30 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | B | 30 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | B | 30 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | B | 30 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | B | 30 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | B | 30 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | B | 45 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | B | 45 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | B | 45 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | E | 40 | 50–150 | 1/10 | 0.4 | 50/5 | 50[4] | 30 | min. 200 | 20/10 | 4.5 | 5 |
| | E | 40 | 100–300 | 1/10 | 0.4 | 50/5 | 50[4] | 30 | min. 250 | 20/10 | 4.5 | 5 |
| | E | 25 | 100–300 | 1/2 | 0.4 | 50/5 | 50[3] | 20 | min. 250 | 20/10 | 4.5 | 5 |
| | E | 40 | 50–150 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 150 | 10/20 | 8.5 | 5 |
| | E | 40 | 100–300 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 200 | 10/20 | 8.5 | 5 |
| | E | 40 | 100–300 | 10/150 | 1.6 | 500/50 | 20[3] | 50 | min. 200 | 20/50 | 8 | 10 |
| | E | 60 | 100–300 | 10/150 | 1.6 | 500/50 | 10[3] | 50 | min. 200 | 20/50 | 8 | 10 |

[1]) Low Noise Type
[2]) Extremely Low Noise Type
[3]) $-I_{CBO}$
[4]) $-I_{CEV}$ at $-V_{EB} = 3$ V
[5]) $-I_{CEV}$ at $-V_{EB} = 0.4$ V

(Plastic Package TO-236)

| Type | Marking Code | $-V_{CEO}$ | $h_{FE}$ | at $-V_{CE}/-I_C$ | $-V_{CEsat}$ | at $-I_C/-I_B$ | $-I_{CES}$ | at $-V_{CE}$ | $f_T$ | at $-V_{CE}/-I_C$ | $C_{ob}$ | at $-V_{CB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | | V/mA | max. V | mA/mA | max. nA | V | MHz | V/mA | max. pF | V |
| | 5A | 45 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | 12 | 10 |
| | 5B | 45 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | 12 | 10 |
| | 5C | 45 | 250–600 | 1/100 | 0.7 | 500/50 | 100 | 45 | 100 | 5/10 | 12 | 10 |
| | 5E | 25 | 100–250 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | 12 | 10 |
| | 5F | 25 | 160–400 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | 12 | 10 |
| | 5G | 25 | 250–600 | 1/100 | 0.7 | 500/50 | 100 | 25 | 100 | 5/10 | 12 | 10 |
| | 3A | 65 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 80 | 150 | 5/10 | 6 | 10 |
| | 3B | 65 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 80 | 150 | 5/10 | 6 | 10 |
| | 3E | 45 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6 | 10 |
| | 3F | 45 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6 | 10 |
| | 3G | 45 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6 | 10 |
| | 3J | 30 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6 | 10 |
| | 3K | 30 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6 | 10 |
| | 3L | 30 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6 | 10 |
| | 4A | 30 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6 | 10 |
| | 4B | 30 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6 | 10 |
| | 4C | 30 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 30 | 150 | 5/10 | 6 | 10 |
| | 4E | 45 | 110–220 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6 | 10 |
| | 4F | 45 | 200–450 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6 | 10 |
| | 4G | 45 | 420–800 | 5/2 | 0.65 | 100/5 | 15 | 50 | 150 | 5/10 | 6 | 10 |
| | BA | 32 | 120–220 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 180 | 5/10 | 6 | 10 |
| | BB | 32 | 180–310 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 180 | 5/10 | 6 | 10 |
| | BC | 32 | 250–460 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 180 | 5/10 | 6 | 10 |
| | BD | 32 | 380–630 | 5/2 | 0.55 | 50/1.25 | 20 | 32 | 180 | 5/10 | 6 | 10 |
| | BG | 45 | 120–220 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 180 | 5/10 | 6 | 10 |
| | BH | 45 | 180–310 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 180 | 5/10 | 6 | 10 |
| | BJ | 45 | 250–460 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 180 | 5/10 | 6 | 10 |
| | BK | 45 | 380–630 | 5/2 | 0.55 | 50/1.25 | 20 | 45 | 180 | 5/10 | 6 | 10 |
| | 5P | 40 | 100–300 | 10/150 | 1.6 | 500/50 | 20[3] | 50 | min. 200 | 20/50 | 8 | 10 |
| | 5R | 60 | 100–300 | 10/150 | 1.6 | 500/50 | 20[3] | 50 | min. 200 | 20/50 | 8 | 10 |
| | 3M | 40 | 50–150 | 1/10 | 0.4 | 50/5 | 50[4] | 30 | min. 200 | 20/10 | 4.5 | 5 |
| | 3N | 40 | 100–300 | 1/10 | 0.4 | 50/5 | 50[4] | 30 | min. 250 | 20/10 | 4.5 | 5 |
| | 3R | 25 | 120–360 | 1/2 | 0.4 | 50/5 | 50[3] | 20 | min. 250 | 20/10 | 4.5 | 5 |
| | 5T | 40 | 50–150 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 150 | 10/20 | 8.5 | 5 |
| | 5U | 40 | 100/300 | 1/150 | 0.75 | 500/50 | 100[5] | 35 | min. 200 | 10/20 | 8.5 | 5 |

Normally, the transistors BC807, BC808 and BC856 to BC860 have the following pin configuration: 1 = collector, 2 = base, 3 = emitter. They are also available with inverted configuration: 1 = collector, 2 = emitter, 3 = base, this being indicated by the suffix "R" next to the type designation and the marking code. Example: type BC856AR is indicated as 3AR.

The transistors IMBT2907, IMBT2907A, IMBT3905, IMBT3906, IMBT4126, IMBT4402, IMBT4403 have the following pin configuration: 1 = collector, 2 = base, 3 = emitter.

Normally, the transistors BCW61 to BCX71 have the following pin configuration: 1 = collector, 2 = base, 3 = emitter. These types are also available with inverted configuration: 1 = collector, 2 = emitter, 3 = base. The type designation and marking is the following.

| Type | Marking |
|---|---|
| BCW61RA | BO |
| BCW61RB | BP |
| BCW61RC | BR |
| BCW61RD | BS |
| | |
| BCX71RG | BU |
| BCX71RH | BW |
| BCX71RJ | BX |
| BCX71RK | BY |

[1]) Low Noise Type
[2]) Extremely Low Noise Type
[3]) $-I_{CBO}$
[4]) $-I_{CEV}$ at $-V_{EB} = 3$ V
[5]) $-I_{CEV}$ at $-V_{EB} = 0.4$ V

# NPN AND PNP TRANSISTORS

(Plastic Package TO-92 D)

| Type | Pin Config. | $V_{CEO}$ | $h_{FE}$ | at $V_{CE}/I_C$ | $V_{CEsat}$ | at $I_C/I_B$ | $I_{CES}$ | at $V_{CE}$ | $f_T$ | at $V_{CE}/I_C$ | $C_{ob}$ | at $V_{CB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | | V/mA | max. V | mA/mA | max. nA | V | min. MHz | V/mA | max. pF | V |
| | D | 25 | 90–180 | 5/1 | 0.6 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | D | 25 | 135–270 | 5/1 | 0.6 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | D | 25 | 200–400 | 5/1 | 0.6 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | D | 25 | 300–600 | 5/1 | 0.6 | 100/5 | 15 | 30 | 150 | 5/10 | 6.0 | 10 |
| | D | 45 | 90–180 | 5/1 | 0.6 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | D | 45 | 135–270 | 5/1 | 0.6 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | D | 45 | 200–400 | 5/1 | 0.6 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |
| | D | 45 | 300–600 | 5/1 | 0.6 | 100/5 | 15 | 50 | 150 | 5/10 | 6.0 | 10 |

(Plastic Package TO-92 D)

| Type | Pin Config. | $-V_{CEO}$ | $h_{FE}$ | at $-V_{CE}/-I_C$ | $-V_{CEsat}$ | at $-I_C/-I_B$ | $-I_{CES}$ | at $-V_{CE}$ | $f_T$ | at $-V_{CE}/-I_C$ | $C_{ob}$ | at $-V_{CB}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Volts | | V/mA | max. V | mA/mA | max. nA | V | typ. MHz | V/mA | max. pF | V |
| | D | 30 | 90–180 | 5/1 | 0.65 | 100/5 | 15 | 25 | 130 | 5/10 | 6.0 | 10 |
| | D | 30 | 135–270 | 5/1 | 0.65 | 100/5 | 15 | 25 | 130 | 5/10 | 6.0 | 10 |
| | D | 30 | 200–400 | 5/1 | 0.65 | 100/5 | 15 | 25 | 130 | 5/10 | 6.0 | 10 |
| | D | 30 | 300–600 | 5/1 | 0.65 | 100/5 | 15 | 30 | 130 | 5/10 | 6.0 | 10 |
| | D | 50 | 90–180 | 5/1 | 0.65 | 100/5 | 15 | 45 | 130 | 5/10 | 6.0 | 10 |
| | D | 50 | 135–270 | 5/1 | 0.65 | 100/5 | 15 | 45 | 130 | 5/10 | 6.0 | 10 |
| | D | 50 | 200–400 | 5/1 | 0.65 | 100/5 | 15 | 45 | 130 | 5/10 | 6.0 | 10 |
| | D | 50 | 300–600 | 5/1 | 0.65 | 100/5 | 15 | 45 | 130 | 5/10 | 6.0 | 10 |

Enhancement-Mode MOSFETs featuring high input impedance, high power gain, fast switching times, CMOS compatibility, no second breakdown, no thermal runaway.

with plastic package 10D3 according to DIN 41870 (≈TO-92). On special request, these transistors will also be produced with TO-18 pin configuration.

| Type | Pin Config. | Maximum Drain-Source Voltage | Maximum Continuous Drain Current | Max. Power Dissipation at $T_C = 25$ °C | Gate Threshold Voltage at $V_{GS} = V_{DS}$, $I_D = 1$ mA | | | Drain-Source ON Resistance [1] | | | | Gate-Body Leakage Current at $V_{GS} = 15$ V, $V_{DS} = 0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | at $V_{GS}$ | and $I_D$ | $I_{GSS}$ |
| | | Volts | Amps | Watts | Volts min. | typ. | max. | Ohms typ. | max. | Volts | Amps | max. Nanoamps |
| | A | 200 | 0.12 | 0.83 | – | 1.8 | 3.0 | 18 | 28 | 2.8 | 0.02 | 10 |
| | A | 200 | 0.23 | 0.83 | – | 1.5 | 2.5 | 5.5 | 8.0 | 2.8 | 0.10 | 10 |
| | A | 170 | 0.2 | 0.83 | – | 1.5 | 2.5 | 5.5 | 10 | 2.8 | 0.10 | 10 |
| | A | 60 | 0.3 | 0.83 | 0.8 | 2.0 | 3.0 | 3.5 | 5.0 | 10 | 0.20 | 10 |
| | B | 200 | 0.25 | 0.83 | – | 1.5 | 2.5 | 4.5 | 7.0 | 5 | 0.10 | 10 |

[1]) Pulse Test Width – 80 μs; Pulse Duty Factor 1%

Enhancement-Mode MOSFETs featuring high input impedance, high power gain, fast switching times, CMOS compatibility, no second breakdown, no thermal runaway.

with plastic package 10D3 according to DIN 41870 (≈TO-92). On special request, these transistors will also be produced with TO-18 pin configuration.

| Type | Pin Config. | Maximum Drain-Source Voltage | Maximum Continuous Drain Current | Max. Power Dissipation at $T_C = 25$ °C | Gate Threshold Voltage at $V_{GS} = V_{DS}$, $-I_D = 1$ mA | | | Drain-Source ON Resistance [1] | | | | Gate-Body Leakage Current at $-V_{GS} = 15$ V, $V_{DS} = 0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | at $V_{GS}$ | and $I_D$ | $I_{GSS}$ |
| | | Volts | Amps | Watts | Volts min. | typ. | max. | Ohms typ. | max. | Volts | Amps | max. Nanoamps |
| | B | –200 | –0.18 | 0.83 | – | –2.8 | –4.0 | 7.0 | 14 | –10 | –0.10 | –10 |
| | A | –200 | –0.2 | 0.83 | – | –2.8 | –4.0 | 7.0 | 14 | –10 | –0.10 | –10 |
| | A | –170 | –0.2 | 0.83 | – | –2.8 | –4.0 | 7.0 | 14 | –10 | –0.10 | –10 |
| | A | –45 | –0.18 | 0.83 | –1.0 | –2.8 | –3.5 | 9.0 | 14 | –10 | –0.20 | –20 |

[1]) Pulse Test Width – 80 μs; Pulse Duty Factor 1%

in DO-35 Package

| Type | Peak Inv. Voltage PIV | Max. Aver. Rectified Current $I_0$ | Power Dissipation at 25 °C | Junction Temperature $T_j$ | Forward Voltage Drop $V_F$ | | Reverse Current $I_R$ | | Reverse Recovery Time | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | at $I_F$ | | at $V_R$ | | |
| | Volts | mA | max. mW | max. °C | max. V | mA | max. nA | Volts | $t_{rr}$ ns | Conditions |
| | 20 | 150 | 300 | 150 | 1.0 | 80 | 50 | 10 | 100 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |
| | 25 | 200 | 400 | 175 | 1.0 | 100 | 100 | 20 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 60 | 200 | 400 | 175 | 1.0 | 100 | 100 | 50 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 120 | 200 | 400 | 175 | 1.0 | 100 | 100 | 100 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 200 | 200 | 400 | 175 | 1.0 | 100 | 100 | 150 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 250 | 200 | 400 | 175 | 1.0 | 100 | 100 | 200 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 35 | 150 | 500 | 200 | 1.0 | 30 | 100 | 25 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$ to $I_R = 1$ mA |
| | 75 | 150 | 500 | 200 | 1.0 | 100 | 100 | 50 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$ to $I_R = 1$ mA |
| | 50 | 48 | 500 | 200 | 1.53 | 75 | 200 | 50 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$ to $I_R = 1$ mA |
| | 165 | 200 | 400 | 175 | 1.3 | 100 | 100 | 150 | max. 120 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$, to $I_R = 3$ mA |
| | 150 | 100 | 400 | 175 | 1.0 | 100 | 100 | 120 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$, to $I_R = 3$ mA |
| | | | | | | | | | | |
| | 100 | 75 | 500 | 200 | 1.0 | 10 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 10 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 10 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 50 | 200 | 500 | 200 | 1.0 | 200 | 100 | 50 | max. 4.0 | $I_F = I_R = 10$ to 200 mA, to 0.1 $I_F$ |
| | 75 | 150 | 500 | 200 | 1.0 | 50 | 50 | 50 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, $I_R = 1$ mA |
| | 40 | 150 | 400 | 175 | 0.55 | 0.10 | 50 | 30 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 75 | 150 | 400 | 175 | 0.55 | 0.10 | 50 | 50 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 35 | 150 | 500 | 200 | 1.0 | 30 | 100 | 25 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 20 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 20 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 100 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 100 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 40 | 150 | 400 | 175 | 0.54 | 0.50 | 50 | 30 | max. 4.0 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |
| | 40 | 150 | 400 | 175 | 0.50 | 0.10 | 50 | 30 | max. 10 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |
| | 30 | 150 | 400 | 175 | 0.55 | 0.01 | 50 | 20 | – | – |
| | 75 | 150 | 400 | 175 | 1.0 | 10 | 100 | 50 | max. 4.0 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |

The following types are also available to specification **CECC 50001-024**: BAV17, BAV18, BAV19, BAV20 and BAV21.
The following types are also available to specification **CECC 50001-023**: 1N4148, 1N4149, 1N4447, 1N4448 and 1N4449.

**CECC** = Cenelec Electronic Components Committee,
**CENELEC** = European Committee for Electrotechnical Standardization.

in MiniMELF Package

| Type | Peak Inv. Voltage PIV | Max. Aver. Rectified Current $I_0$ | Power Dissipation at 25 °C | Junction Temperature $T_j$ | Forward Voltage Drop $V_F$ | | Reverse Current $I_R$ | | Reverse Recovery Time | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | at $I_F$ | | at $V_R$ | | |
| | Volts | mA | max. mW | max. °C | max. V | mA | max. nA | Volts | $t_{rr}$ ns | Conditions |
| | 60 | 200 | 400 | 175 | 1.0 | 100 | 100 | 50 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 120 | 200 | 400 | 175 | 1.0 | 100 | 100 | 100 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 200 | 200 | 400 | 175 | 1.0 | 100 | 100 | 150 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 250 | 200 | 400 | 175 | 1.0 | 100 | 100 | 200 | max. 50 | $I_F = I_R = 30$ mA, $R_L = 100\,\Omega$ to $I_R = 3$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 10 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 10 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 50 | 200 | 500 | 200 | 1.0 | 200 | 100 | 50 | max. 4.0 | $I_F = I_R = 10$ to 200 mA, to 0.1 $I_F$ |
| | 75 | 150 | 500 | 200 | 1.0 | 50 | 50 | 50 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 40 | 150 | 400 | 175 | 0.55 | 0.10 | 50 | 30 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 75 | 150 | 400 | 175 | 0.55 | 0.10 | 50 | 50 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 35 | 150 | 500 | 200 | 1.0 | 30 | 100 | 25 | max. 2.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 20 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 20 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 100 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 100 | 150 | 500 | 200 | 1.0 | 100 | 25 | 20 | max. 4.0 | $I_F = 10$ mA, $V_R = 6$ V, $R_L = 100\,\Omega$, to $I_R = 1$ mA |
| | 40 | 150 | 400 | 175 | 0.54 | 0.50 | 50 | 30 | max. 4.0 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |
| | 40 | 150 | 400 | 175 | 0.50 | 0.10 | 50 | 30 | max. 10 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |
| | 30 | 150 | 400 | 175 | 0.55 | 0.01 | 50 | 20 | – | – |
| | 75 | 150 | 400 | 175 | 1.0 | 10 | 100 | 50 | max. 4.0 | $I_F = I_R = 10$ mA, to $I_R = 1$ mA |

# SOLID STATE TUNER COMPONENTS

(delivered in matched sets)

| Type | Package | Capacitance | | | Capacitance Ratio | | | | Series Resistance | | | | Reverse Current | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | min. pF | max. pF | at $V_R$ V | min. | max. | at V $V_R$ = to | V | Ω typ. | Ω max. | at f MHz | and C pF | max. nA | at $V_R$ V |
| | TO-236 | 42 | 43.5 | 2 | 1.65 | 1.75 | 2 | 8 | – | 0.4 | 100 | 38 | 20 | 10 |
| | TO-236 | 43 | 44.5 | 2 | 1.65 | 1.75 | 2 | 8 | – | 0.4 | 100 | 38 | 20 | 10 |
| | TO-236 | 44 | 45.5 | 2 | 1.65 | 1.75 | 2 | 8 | – | 0.4 | 100 | 38 | 20 | 10 |
| | TO-236 | 45 | 46.5 | 2 | 1.65 | 1.75 | 2 | 8 | – | 0.4 | 100 | 38 | 20 | 10 |
| | TO-236 | 46 | 47.5 | 2 | 1.65 | 1.75 | 2 | 8 | – | 0.4 | 100 | 38 | 20 | 10 |
| | TO-236 | 440 | 600 | 1 | 15 | – | 1 | 9 | – | – | – | – | 30 | 10 |
| | ≈60A2 | 0.9 | 1.2 | 28 | 8.0 | 9 | 1 | 28 | – | 1.2 | 470 | 9 | 30 | 30 |
| | ≈60A2 | 2.0 | 2.29 | 28 | 8.0 | – | 1 | 28 | – | 0.5 | 470 | 14 | 30 | 30 |
| | ≈60A2 | 1.9 | 2.25 | 28 | 9.5 | 15 | 1 | 28 | – | 0.8 | 470 | 14 | 30 | 30 |
| | ≈60A2 | 2.38 | 2.93 | 28 | 12 | – | 1 | 28 | – | 0.8 | 470 | 25 | 30 | 30 |
| | ≈60A2 | 2.7 | 2.9 | 28 | 14.8 | 16.8 | 1 | 28 | – | 0.9 | 330 | 25 | 30 | 28 |
| | ≈60A2 | 3.15 | 3.55 | 28 | 19.5 | 25 | 1 | 28 | 0.9 | 1.0 | 300 | 25 | 30 | 30 |

* The types BB404 are dual capacitance diodes with common cathode. Pin 1: Cathode, Pin 2: Anode 1, Pin 3: Anode 2.
** Pins 1 and 2: Cathode, Pin 3: Anode

| Type | Package | Reverse Voltage | Forward Current at $T_A$ = 25 °C | Forward Voltage Drop at $I_F$ = 100 mA | Reverse Current at $V_R$ = 20 V | Forward Dynamic Impedance at f = 50–1000 MHz | | | Series Inductance Directly Across Package | Capacitance at $V_R$ = 3 V, f = 1 MHz |
|---|---|---|---|---|---|---|---|---|---|---|
| | | max. Volts | max. mA | max. Volts | max. nA | typ. Ω | max. Ω | at $I_F$ mA | nH typ. | max. pF |
| | DO-35 | 35 | 100 | 1.0 | 50 | 0.7 | 1.0 | 10 | 2.5 | 1.80 |
| | DO-35 | 35 | 100 | 1.0 | 50 | 0.4 | 0.5 | 10 | 2.5 | 1.80 |
| | DO-35 | 35 | 100 | 1.0 | 50 | – | 0.7 | 3.0 | 2.5 | 1.25 |
| | DO-35 | 35 | 100 | 1.0 | 50 | – | 1.2 | 3.0 | 2.5 | 1.20 |
| | MiniMELF | 35 | 100 | 1.0 | 50 | – | 0.7 | 3.0 | 2.0 | 1.25 |
| | MiniMELF | 35 | 100 | 1.0 | 50 | – | 1.2 | 3.0 | 2.0 | 1.20 |
| | ≈60A2 | 35 | 100 | 1.0 | 50 | – | 0.7 | 3.0 | 2.5 | 1.25 |
| | ≈60A2 | 35 | 100 | 1.0 | 50 | – | 1.2 | 3.0 | 2.5 | 1.20 |

in DO-35 Package

for general purpose applications with low forward voltage drop and very fast switching times.
Using the type designations **LL101A, LL103A** and so on, these Schottky Barrier diodes are available in the MiniMELF package with the same electrical characteristics.

| Type | Peak Inv. Voltage PIV | Power Dissipation at 25 °C | Junction and Storage Temp. | Forward Voltage Drop $V_F$ at $I_F$ | | | | Reverse Current $I_R$ at $V_R$ | | Capacitance at $V_F = V_R = 0$, f = 1 MHz | Reverse Recovery Time $t_{rr}$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Volts | max. mW | max. °C | max. V | at mA | max. V | at mA | max. µA | at V | max. pF | max. ns | Conditions |
| | 60 | 400 | 200 | 0.41 | 1 | 1.0 | 15 | 0.2 | 50 | 2.0 | 1 | $I_F = I_R = 5$ mA to 0.1 $I_R$ |
| | 50 | 400 | 200 | 0.40 | 1 | 0.95 | 15 | 0.2 | 40 | 2.1 | 1 | $I_F = I_R = 5$ mA to 0.1 $I_R$ |
| | 40 | 400 | 200 | 0.39 | 1 | 0.90 | 15 | 0.2 | 30 | 2.2 | 1 | $I_F = I_R = 5$ mA to 0.1 $I_R$ |
| | 40 | 400 | 125 | 0.37 | 20 | 0.6 | 200 | 5.0 | 30 | 50 | 10 | $I_F = I_R = 200$ mA to 0.1 $I_R$ |
| | 30 | 400 | 125 | 0.37 | 20 | 0.6 | 200 | 5.0 | 20 | 50 | 10 | $I_F = I_R = 200$ mA to 0.1 $I_R$ |
| | 20 | 400 | 125 | 0.37 | 20 | 0.6 | 200 | 5.0 | 10 | 50 | 10 | $I_F = I_R = 200$ mA to 0.1 $I_R$ |

*JEDEC Equivalent:

in Plastic Package P2 or P3

for clipping peaks in telephone circuits and for general applications. All parameters are valid for both current directions. Any diode destroyed by overload shows a short-circuit caused by through-alloying the junction.

| Type | Dwg. No. | Zener Voltage Range at $I_Z = 5$ mA | Permissible Pulse Current | | Voltage Drop | | Temperature Coefficient | Reverse Voltage | Capacitance |
|---|---|---|---|---|---|---|---|---|---|
| | | | at Pulses 8/20 | at Pulses 10/1000 | at Pulses 8/20 | at Pulses 10/1000 | at $I_Z = 5$ mA | at $I_R = 5$ µA | at $V_R = 0$ |
| | | Volts | max. Amps | max. Amps | max. Volts | max. Volts | x $10^{-4}$/°C | min. Volts | typ. pF |
| | P2 | 13–19 | 300 | 30 | 30 | 25 | 4–10 | 9.6 | 1800 |
| | P2 | 18–26 | 200 | 20 | 38 | 33 | 4–10 | 13.2 | 1400 |
| | P2 | 30–42 | 130 | 13 | 60 | 53 | 5–11 | 21.6 | 700 |
| | P2 | 52–72 | 80 | 8 | 105 | 90 | 6–12 | 37.2 | 450 |
| | P2 | 63–87 | 68 | 6.8 | 122 | 110 | 6–12 | 45 | 350 |
| | P2 | 76–106 | 56 | 5.6 | 146 | 132 | 6–12 | 54.6 | 300 |
| | P2 | 92–128 | 45 | 4.5 | 178 | 162 | 6–12 | 66 | 250 |
| | P2 | 135–185 | 30 | 3 | 255 | 235 | 6–12 | 96 | 200 |
| | P3 | 13–19 | 200 | 20 | 35 | 30 | 4–10 | 9.6 | 1200 |
| | P3 | 18–26 | 130 | 13 | 45 | 38 | 4–10 | 13.2 | 900 |
| | P3 | 30–42 | 90 | 9 | 75 | 65 | 5–11 | 21.6 | 500 |
| | P3 | 52–72 | 60 | 6 | 125 | 110 | 6–12 | 37.2 | 300 |
| | P3 | 63–87 | 50 | 5 | 145 | 132 | 6–12 | 45 | 250 |
| | P3 | 76–106 | 40 | 4 | 175 | 162 | 6–12 | 54.6 | 200 |
| | P3 | 92–128 | 30 | 3 | 210 | 195 | 6–12 | 66 | 170 |
| | P3 | 135–185 | 20 | 2 | 305 | 285 | 6–12 | 96 | 150 |

in DO-35 Package ($T_A$ = 25 °C)

Using the type designations **ZMM5225, ZMM5226** and so on, these Zener diodes are available in the MiniMELF package with the same electrical characteristics.

| Type | Nominal Zener Voltage $V_Z$ at $I_{ZT}$* | Test Current $I_{ZT}$ | Maximum Zener Impedance $Z_{ZT}$ at $I_{ZT}$ | Maximum Zener Impedance $Z_{ZK}$ at $I_{ZK}$ = 0.25 mA | Typical Temperature Coefficient | Maximum Reverse Leakage Current $I_R$ | Test-Voltage Suffix A | Suffix B | Maximum Regulator Current $I_{ZM}$ |
|---|---|---|---|---|---|---|---|---|---|
| | Volts | mA | Ohms | Ohms | %/°C | µA | Volts | Volts | mA |
| | 3.0 | 20 | 29 | 1600 | −0.075 | 50 | 0.95 | 1.0 | 152 |
| | 3.3 | 20 | 28 | 1600 | −0.070 | 25 | 0.95 | 1.0 | 138 |
| | 3.6 | 20 | 24 | 1700 | −0.065 | 15 | 0.95 | 1.0 | 126 |
| | 3.9 | 20 | 23 | 1900 | −0.060 | 10 | 0.95 | 1.0 | 115 |
| | 4.3 | 20 | 22 | 2000 | −0.055 | 5 | 0.95 | 1.0 | 106 |
| | 4.7 | 20 | 19 | 1900 | ±0.030 | 5 | 1.9 | 2.0 | 97 |
| | 5.1 | 20 | 17 | 1600 | ±0.030 | 5 | 1.9 | 2.0 | 89 |
| | 5.6 | 20 | 11 | 1600 | +0.038 | 5 | 2.9 | 3.0 | 81 |
| | 6.0 | 20 | 7 | 1600 | +0.038 | 5 | 3.3 | 3.5 | 76 |
| | 6.2 | 20 | 7 | 1000 | +0.045 | 5 | 3.8 | 4.0 | 73 |
| | 6.8 | 20 | 5 | 750 | +0.050 | 3 | 4.8 | 5.0 | 67 |
| | 7.5 | 20 | 6 | 500 | +0.058 | 3 | 5.7 | 6.0 | 61 |
| | 8.2 | 20 | 8 | 500 | +0.062 | 3 | 6.2 | 6.5 | 55 |
| | 8.7 | 20 | 8 | 600 | +0.065 | 3 | 6.2 | 6.5 | 52 |
| | 9.1 | 20 | 10 | 600 | +0.068 | 3 | 6.7 | 7.0 | 50 |
| | 10 | 20 | 17 | 600 | +0.075 | 3 | 7.6 | 8.0 | 45 |
| | 11 | 20 | 22 | 600 | +0.076 | 2 | 8.0 | 8.4 | 41 |
| | 12 | 20 | 30 | 600 | +0.077 | 1 | 8.7 | 9.1 | 38 |
| | 13 | 9.5 | 13 | 600 | +0.079 | 0.5 | 9.4 | 9.9 | 35 |
| | 14 | 9.0 | 15 | 600 | +0.082 | 0.1 | 9.5 | 10 | 32 |
| | 15 | 8.5 | 16 | 600 | +0.082 | 0.1 | 10.5 | 11 | 30 |
| | 16 | 7.8 | 17 | 600 | +0.083 | 0.1 | 11.4 | 12 | 28 |
| | 17 | 7.4 | 19 | 600 | +0.084 | 0.1 | 12.4 | 13 | 27 |
| | 18 | 7.0 | 21 | 600 | +0.085 | 0.1 | 13.3 | 14 | 25 |
| | 19 | 6.6 | 23 | 600 | +0.086 | 0.1 | 13.3 | 14 | 24 |
| | 20 | 6.2 | 25 | 600 | +0.086 | 0.1 | 14.3 | 15 | 23 |
| | 22 | 5.6 | 29 | 600 | +0.087 | 0.1 | 16.2 | 17 | 21 |
| | 24 | 5.2 | 33 | 600 | +0.087 | 0.1 | 17.1 | 18 | 19.1 |
| | 25 | 5.0 | 35 | 600 | +0.089 | 0.1 | 18.1 | 19 | 18.2 |
| | 27 | 4.6 | 41 | 600 | +0.090 | 0.1 | 20 | 21 | 16.8 |
| | 28 | 4.5 | 44 | 600 | +0.091 | 0.1 | 20 | 21 | 16.2 |
| | 30 | 4.2 | 49 | 600 | +0.091 | 0.1 | 22 | 23 | 15.1 |
| | 33 | 3.8 | 58 | 700 | +0.092 | 0.1 | 24 | 25 | 13.8 |
| | 36 | 3.4 | 70 | 700 | +0.093 | 0.1 | 26 | 27 | 12.6 |
| | 39 | 3.2 | 80 | 800 | +0.094 | 0.1 | 29 | 30 | 11.6 |
| | 43 | 3.0 | 93 | 900 | +0.095 | 0.1 | 31 | 33 | 10.6 |
| | 47 | 2.7 | 105 | 1000 | +0.095 | 0.1 | 34 | 36 | 9.7 |
| | 51 | 2.5 | 125 | 1100 | +0.096 | 0.1 | 37 | 39 | 8.9 |

Standard Voltage Tolerance is ±20%. Add Suffix "A" for ±10% Tolerance and Suffix "B" for ±5% Tolerance.
Other Tolerances, Non-Standard and Higher Zener Voltages Upon Request.

*Measured under thermal equilibrium and DC test conditions.

in DO-35 Package ($T_A$ = 25 °C)

| Type | Zener Voltage Range at $I_Z$ = 5 mA* | Maximum Zener Impedance at $I_Z$ = 5 mA $Z_{ZT}$ | Maximum Zener Impedance at $I_Z$ = 1 mA $Z_{ZK}$ | Typical Temperature Coefficient | Maximum Reverse Leakage Current $I_R$ | Test Voltage | Maximum Regulator Current $I_{ZM}$ |
|---|---|---|---|---|---|---|---|
| | $V_Z$ Volts | Ohms | Ohms | %/°C | µA | Volts | mA |
| | 0.73–0.83 | 8 | 600 | −0.250 | – | – | – |
| | 2.5–2.9 | 85 | 600 | −0.070 | 10 | 1.0 | 135 |
| | 2.8–3.2 | 85 | 600 | −0.070 | 4 | 1.0 | 125 |
| | 3.1–3.5 | 85 | 600 | −0.065 | 2 | 1.0 | 115 |
| | 3.4–3.8 | 85 | 600 | −0.060 | 2 | 1.0 | 105 |
| | 3.7–4.1 | 85 | 600 | −0.050 | 2 | 1.0 | 95 |
| | 4.0–4.6 | 75 | 600 | −0.025 | 1 | 1.0 | 90 |
| | 4.4–5.0 | 60 | 600 | −0.010 | 0.5 | 1.0 | 85 |
| | 4.8–5.4 | 35 | 550 | +0.015 | 0.1 | 1.0 | 80 |
| | 5.2–6.0 | 25 | 450 | +0.025 | 0.1 | 1.0 | 70 |
| | 5.8–6.6 | 10 | 200 | +0.035 | 0.1 | 2.0 | 64 |
| | 6.4–7.2 | 8 | 150 | +0.045 | 0.1 | 3.0 | 58 |
| | 7.0–7.9 | 7 | 50 | +0.050 | 0.1 | 5.0 | 53 |
| | 7.7–8.7 | 7 | 50 | +0.050 | 0.1 | 6.0 | 47 |
| | 8.5–9.6 | 10 | 50 | +0.060 | 0.1 | 7.0 | 43 |
| | 9.4–10.6 | 15 | 70 | +0.070 | 0.1 | 7.5 | 40 |
| | 10.4–11.6 | 20 | 70 | +0.070 | 0.1 | 8.5 | 36 |
| | 11.4–12.7 | 20 | 90 | +0.070 | 0.1 | 9.0 | 32 |
| | 12.4–14.1 | 26 | 110 | +0.070 | 0.1 | 10 | 29 |
| | 13.8–15.6 | 30 | 110 | +0.070 | 0.1 | 11 | 27 |
| | 15.3–17.1 | 40 | 170 | +0.070 | 0.1 | 12 | 24 |
| | 16.8–19.1 | 50 | 170 | +0.070 | 0.1 | 14 | 21 |
| | 18.8–21.2 | 55 | 220 | +0.070 | 0.1 | 15 | 20 |
| | 20.8–23.3 | 55 | 220 | +0.070 | 0.1 | 17 | 18 |
| | 22.8–25.6 | 80 | 220 | +0.080 | 0.1 | 18 | 16 |
| | 25.1–28.9 | 80 | 220 | +0.080 | 0.1 | 20 | 14 |
| | 28–32 | 80 | 220 | +0.080 | 0.1 | 22 | 13 |
| | 31–35 | 80 | 220 | +0.080 | 0.1 | 24 | 12 |
| | 34–38 | 80 | 220 | +0.080 | 0.1 | 27 | 11 |
| | 37–41** | 90** | 500*** | +0.080 | 0.1 | 28 | 10 |
| | 40–46** | 90** | 600*** | +0.080 | 0.1 | 32 | 9.2 |
| | 44–50** | 110** | 700*** | +0.080 | 0.1 | 35 | 8.5 |
| | 48–54** | 110** | 700*** | +0.080 | 0.1 | 38 | 7.8 |

Standard Voltage Tolerance is ±5%. Other Tolerances, Non-Standard and Higher Zener Voltages Upon Request.
The BZX55-C0V8 is a silicon diode operated in forward direction. Hence, the cathode terminal is to be connected to the negative pole of the supply.

These types are also available to specification **NEN CECC 50.005.005.**

**CECC** = Cenelec Electronic Components Committee,
**CENELEC** = European Committee for Electrotechnical Standardization.

*Measured with pulses tp = 20 ms.
**at $I_Z$ = 2.5 mA
***at $I_Z$ = 0.5 mA

in TO-236 Package ($T_A$ = 25 °C)

| Type | Marking Code | Zener Voltage Range $V_Z$ at $I_{ZT}$* | Maximum Zener Impedance $Z_{ZT}$ | at $I_{ZT}$ | $Z_{ZK}$ | at $I_{ZK}$ | Typical Temperature Coefficient at $I_Z$ = 5 mA | Maximum Reserve Leakage Current $-I_R$ | at $V_R$ |
|---|---|---|---|---|---|---|---|---|---|
| | | $V_Z$ Volts | Ohms | mA | Ohms | mA | %/°C | μA | Volts |
| | Z12 | 2.5–2.9 | 100 | 5 | 600 | 1 | −0.065 | 20 | 1 |
| | Z13 | 2.8–3.2 | 100 | 5 | 600 | 1 | −0.060 | 10 | 1 |
| | Z14 | 3.1–3.5 | 95 | 5 | 600 | 1 | −0.055 | 5 | 1 |
| | Z15 | 3.4–3.8 | 95 | 5 | 600 | 1 | −0.055 | 5 | 1 |
| | Z16 | 3.7–4.1 | 90 | 5 | 600 | 1 | −0.050 | 3 | 1 |
| | Z17 | 4.0–4.6 | 90 | 5 | 600 | 1 | −0.035 | 3 | 1 |
| | Z1 | 4.4–5.0 | 80 | 5 | 500 | 1 | −0.015 | 3 | 2 |
| | Z2 | 4.8–5.4 | 60 | 5 | 480 | 1 | +0.005 | 2 | 2 |
| | Z3 | 5.2–6.0 | 40 | 5 | 400 | 1 | +0.020 | 1 | 2 |
| | Z4 | 5.8–6.6 | 10 | 5 | 150 | 1 | +0.030 | 3 | 4 |
| | Z5 | 6.4–7.2 | 15 | 5 | 80 | 1 | +0.045 | 2 | 4 |
| | Z6 | 7.0–7.9 | 15 | 5 | 80 | 1 | +0.050 | 1 | 5 |
| | Z7 | 7.7–8.7 | 15 | 5 | 80 | 1 | +0.055 | 0.7 | 5 |
| | Z8 | 8.5–9.6 | 15 | 5 | 100 | 1 | +0.065 | 0.5 | 6 |
| | Z9 | 9.4–10.6 | 20 | 5 | 150 | 1 | +0.065 | 0.2 | 7 |
| | Y1 | 10.4–11.6 | 20 | 5 | 150 | 1 | +0.070 | 0.1 | 8 |
| | Y2 | 11.4–12.7 | 25 | 5 | 150 | 1 | +0.075 | 0.1 | 8 |
| | Y3 | 12.4–14.1 | 30 | 5 | 170 | 1 | +0.080 | 0.1 | 8 |
| | Y4 | 13.8–15.6 | 30 | 5 | 200 | 1 | +0.080 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y5 | 15.3–17.1 | 40 | 5 | 200 | 1 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y6 | 16.8–19.1 | 45 | 5 | 225 | 1 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y7 | 18.8–21.2 | 55 | 5 | 225 | 1 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y8 | 20.8–23.3 | 55 | 5 | 250 | 1 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y9 | 22.8–25.6 | 70 | 5 | 250 | 1 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y10 | 25.1–28.9 | 80 | 2 | 300 | 0.5 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y11 | 28–32 | 80 | 2 | 300 | 0.5 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y12 | 31–35 | 80 | 2 | 325 | 0.5 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y13 | 34–38 | 90 | 2 | 350 | 0.5 | +0.090 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y14 | 37–41 | 130 | 2 | 350 | 0.5 | +0.110 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y15 | 40–46 | 150 | 2 | 375 | 0.5 | +0.110 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y16 | 44–50 | 170 | 2 | 375 | 0.5 | +0.110 | 0.05 | 0.7 $V_{Znom.}$ |
| | Y17 | 48–54 | 180 | 2 | 400 | 0.5 | +0.110 | 0.05 | 0.7 $V_{Znom.}$ |

Standard Voltage Tolerance is 5%.

* Measured with pulses tp = 20 ms.

in DO-35 Package ($T_A$ = 25 °C)

| Type | Zener Voltage Range* | | Maximum Zener Impedance | | | | Typical Temperature Coefficient at $I_Z$ = 5 mA | Min. Reverse Voltage at $I_R$ = 0.1 µA | Maximum Regulator Current |
|---|---|---|---|---|---|---|---|---|---|
| | | at $I_{ZT}$ | $Z_{ZT}$ | at $I_{ZT}$ | $Z_{ZK}$ | at $I_{ZK}$ | | $V_R$ | $I_{ZM}$ |
| | $V_Z$ Volts | mA | Ohms | mA | Ohms | mA | %/°C | Volts | mA |
| | 0.7–0.8 | 5 | 8 | 5 | 50 | 1 | −0.24 | – | 340 |
| | 2.5–2.9 | 5 | 83 | 5 | 500 | 1 | −0.065 | – | 160 |
| | 2.8–3.2 | 5 | 95 | 5 | 500 | 1 | −0.060 | – | 140 |
| | 3.1–3.5 | 5 | 95 | 5 | 500 | 1 | −0.055 | – | 130 |
| | 3.4–3.8 | 5 | 95 | 5 | 500 | 1 | −0.055 | – | 120 |
| | 3.7–4.1 | 5 | 95 | 5 | 500 | 1 | −0.050 | – | 110 |
| | 4.0–4.6 | 5 | 95 | 5 | 500 | 1 | −0.035 | – | 100 |
| | 4.4–5.0 | 5 | 78 | 5 | 500 | 1 | −0.015 | – | 90 |
| | 4.8–5.4 | 5 | 60 | 5 | 480 | 1 | +0.005 | 0.8 | 80 |
| | 5.2–6.0 | 5 | 40 | 5 | 400 | 1 | +0.020 | 1.0 | 70 |
| | 5.8–6.6 | 5 | 10 | 5 | 200 | 1 | +0.030 | 2.0 | 64 |
| | 6.4–7.2 | 5 | 8 | 5 | 150 | 1 | +0.045 | 3.0 | 58 |
| | 7.0–7.9 | 5 | 7 | 5 | 50 | 1 | +0.050 | 5.0 | 53 |
| | 7.7–8.7 | 5 | 7 | 5 | 50 | 1 | +0.055 | 6.0 | 47 |
| | 8.5–9.6 | 5 | 10 | 5 | 50 | 1 | +0.065 | 7.0 | 43 |
| | 9.4–10.6 | 5 | 15 | 5 | 70 | 1 | +0.065 | 7.5 | 40 |
| | 10.4–11.6 | 5 | 20 | 5 | 70 | 1 | +0.070 | 8.5 | 36 |
| | 11.4–12.7 | 5 | 20 | 5 | 90 | 1 | +0.075 | 9.0 | 32 |
| | 12.4–14.1 | 5 | 25 | 5 | 110 | 1 | +0.080 | 10 | 29 |
| | 13.8–15.6 | 5 | 30 | 5 | 110 | 1 | +0.080 | 11 | 27 |
| | 15.3–17.1 | 5 | 40 | 5 | 170 | 1 | +0.090 | 12 | 24 |
| | 16.8–19.1 | 5 | 50 | 5 | 170 | 1 | +0.090 | 14 | 21 |
| | 18.8–21.2 | 5 | 50 | 5 | 220 | 1 | +0.090 | 15 | 20 |
| | 20.8–23.3 | 5 | 55 | 5 | 220 | 1 | +0.090 | 17 | 18 |
| | 22.8–25.6 | 5 | 80 | 5 | 220 | 1 | +0.090 | 18 | 16 |
| | 25.1–28.9 | 5 | 80 | 5 | 250 | 1 | +0.090 | 20 | 14 |
| | 28–32 | 5 | 80 | 5 | 250 | 1 | +0.090 | 22.5 | 13 |
| | 31–35 | 5 | 80 | 5 | 250 | 1 | +0.090 | 25 | 12 |
| | 34–38 | 5 | 90 | 5 | 250 | 1 | +0.090 | 27 | 11 |
| | 37–41 | 5 | 90 | 5 | 300 | 1 | +0.110 | 29 | 10 |
| | 40–46 | 5 | 100 | 5 | 700 | 1 | +0.110 | 32 | 9.2 |
| | 44–50 | 5 | 100 | 5 | 750 | 1 | +0.110 | 35 | 8.5 |
| | 48–54 | 5 | 100 | 5 | 750 | 1 | +0.110 | 38 | 7.8 |

Standard Voltage Tolerance is ±5%. Other Tolerances, Non-Standard and Higher Zener Voltages Upon Request.
The ZPD1 is a silicon diode operated in forward direction. Hence, the cathode terminal is to be connected to the negative pole of the supply.

*Measured with pulses tp = 20 ms.

in MiniMELF Package ($T_A$ = 25 °C)

| Type | Zener Voltage Range* | | Maximum Zener Impedance | | | | Typical Temperature Coefficient at $I_Z$ = 5 mA | Min. Reverse Voltage at $I_R$ = 0.1 µA | Maximum Regulator Current |
|---|---|---|---|---|---|---|---|---|---|
| | | at $I_{ZT}$ | $Z_{ZT}$ | at $I_{ZT}$ | $Z_{ZK}$ | at $I_{ZK}$ | | $V_R$ | $I_{ZM}$ |
| | $V_Z$ Volts | mA | Ohms | mA | Ohms | mA | %/°C | Volts | mA |
| | 0.7–0.8 | 5 | 8 | 5 | 50 | 1 | −0.24 | – | 340 |
| | 2.5–2.9 | 5 | 83 | 5 | 500 | 1 | −0.065 | – | 160 |
| | 2.8–3.2 | 5 | 95 | 5 | 500 | 1 | −0.060 | – | 140 |
| | 3.1–3.5 | 5 | 95 | 5 | 500 | 1 | −0.055 | – | 130 |
| | 3.4–3.8 | 5 | 95 | 5 | 500 | 1 | −0.055 | – | 120 |
| | 3.7–4.1 | 5 | 95 | 5 | 500 | 1 | −0.050 | – | 110 |
| | 4.0–4.6 | 5 | 95 | 5 | 500 | 1 | −0.035 | – | 100 |
| | 4.4–5.0 | 5 | 78 | 5 | 500 | 1 | −0.015 | – | 90 |
| | 4.8–5.4 | 5 | 60 | 5 | 480 | 1 | +0.005 | 0.8 | 80 |
| | 5.2–6.0 | 5 | 40 | 5 | 400 | 1 | +0.020 | 1.0 | 70 |
| | 5.8–6.6 | 5 | 10 | 5 | 200 | 1 | +0.030 | 2.0 | 64 |
| | 6.4–7.2 | 5 | 8 | 5 | 150 | 1 | +0.045 | 3.0 | 58 |
| | 7.0–7.9 | 5 | 7 | 5 | 50 | 1 | +0.050 | 5.0 | 53 |
| | 7.7–8.7 | 5 | 7 | 5 | 50 | 1 | +0.055 | 6.0 | 47 |
| | 8.5–9.6 | 5 | 10 | 5 | 50 | 1 | +0.065 | 7.0 | 43 |
| | 9.4–10.6 | 5 | 15 | 5 | 70 | 1 | +0.065 | 7.5 | 40 |
| | 10.4–11.6 | 5 | 20 | 5 | 70 | 1 | +0.070 | 8.5 | 36 |
| | 11.4–12.7 | 5 | 20 | 5 | 90 | 1 | +0.075 | 9.0 | 32 |
| | 12.4–14.1 | 5 | 25 | 5 | 110 | 1 | +0.080 | 10 | 29 |
| | 13.8–15.6 | 5 | 30 | 5 | 110 | 1 | +0.080 | 11 | 27 |
| | 15.3–17.1 | 5 | 40 | 5 | 170 | 1 | +0.090 | 12 | 24 |
| | 16.8–19.1 | 5 | 50 | 5 | 170 | 1 | +0.090 | 14 | 21 |
| | 18.8–21.2 | 5 | 50 | 5 | 220 | 1 | +0.090 | 15 | 20 |
| | 20.8–23.3 | 5 | 55 | 5 | 220 | 1 | +0.090 | 17 | 18 |
| | 22.8–25.6 | 5 | 80 | 5 | 220 | 1 | +0.090 | 18 | 16 |
| | 25.1–28.9 | 5 | 80 | 5 | 250 | 1 | +0.090 | 20 | 14 |
| | 28–32 | 5 | 80 | 5 | 250 | 1 | +0.090 | 22.5 | 13 |
| | 31–35 | 5 | 80 | 5 | 250 | 1 | +0.090 | 25 | 12 |
| | 34–38 | 5 | 90 | 5 | 250 | 1 | +0.090 | 27 | 11 |
| | 37–41 | 5 | 90 | 5 | 300 | 1 | +0.110 | 29 | 10 |
| | 40–46 | 5 | 100 | 5 | 700 | 1 | +0.110 | 32 | 9.2 |
| | 44–50 | 5 | 100 | 5 | 750 | 1 | +0.110 | 35 | 8.5 |
| | 48–54 | 5 | 100 | 5 | 750 | 1 | +0.110 | 38 | 7.8 |

Standard Voltage Tolerance is ±5%. Other Tolerances, Non-Standard and Higher Zener Voltages Upon Request.
The ZMM1 is a silicon diode operated in forward direction. Hence, the cathode terminal is to be connected to the negative pole of the supply.

*Measured with pulses tp = 20 ms.

in DO-41 Package ($T_A$ = 25 °C)

Using the type designations **ZM4729, ZM4730** and so on, these Zener diodes are available in the MELF package with the same electrical characteristics.

| Type | Nominal Zener Voltage $V_Z$ at $I_{ZT}$* | Test Current $I_{ZT}$ | Maximum Zener Impedance | | | Maximum Reverse Leakage Current | | Max. Surge Current 8.3 ms | Maximum Regulator Current |
|---|---|---|---|---|---|---|---|---|---|
| | | | $Z_{ZT}$ at $I_{ZT}$ | $Z_{ZK}$ at $I_{ZK}$ | $I_{ZK}$ | $I_R$ | at $V_R$ | $I_{ZS}$ | $I_{ZM}$ |
| | Volts | mA | Ohms | Ohms | mA | µA | Volts | mA | mA |
| | 3.6 | 69 | 10 | 400 | 1.0 | 100 | 1 | 1260 | 252 |
| | 3.9 | 64 | 9 | 400 | 1.0 | 100 | 1 | 1190 | 234 |
| | 4.3 | 58 | 9 | 400 | 1.0 | 50 | 1 | 1070 | 217 |
| | 4.7 | 53 | 8 | 500 | 1.0 | 10 | 1 | 970 | 193 |
| | 5.1 | 49 | 7 | 550 | 1.0 | 10 | 1 | 890 | 178 |
| | 5.6 | 45 | 5 | 600 | 1.0 | 10 | 2 | 810 | 162 |
| | 6.2 | 41 | 2 | 700 | 1.0 | 10 | 3 | 730 | 146 |
| | 6.8 | 37 | 3.5 | 700 | 1.0 | 10 | 4 | 660 | 133 |
| | 7.5 | 34 | 4 | 700 | 0.5 | 10 | 5 | 605 | 121 |
| | 8.2 | 31 | 4.5 | 700 | 0.5 | 10 | 6 | 550 | 110 |
| | 9.1 | 28 | 5 | 700 | 0.5 | 10 | 7 | 500 | 100 |
| | 10 | 25 | 7 | 700 | 0.25 | 10 | 7.6 | 454 | 91 |
| | 11 | 23 | 8 | 700 | 0.25 | 5 | 8.4 | 414 | 83 |
| | 12 | 21 | 9 | 700 | 0.25 | 5 | 9.1 | 380 | 76 |
| | 13 | 19 | 10 | 700 | 0.25 | 5 | 9.9 | 344 | 69 |
| | 15 | 17 | 14 | 700 | 0.25 | 5 | 11.4 | 304 | 61 |
| | 16 | 15.5 | 16 | 700 | 0.25 | 5 | 12.2 | 285 | 57 |
| | 18 | 14 | 20 | 750 | 0.25 | 5 | 13.7 | 250 | 50 |
| | 20 | 12.5 | 22 | 750 | 0.25 | 5 | 15.2 | 225 | 45 |
| | 22 | 11.5 | 23 | 750 | 0.25 | 5 | 16.7 | 205 | 41 |
| | 24 | 10.5 | 25 | 750 | 0.25 | 5 | 18.2 | 190 | 38 |
| | 27 | 9.5 | 35 | 750 | 0.25 | 5 | 20.6 | 170 | 34 |
| | 30 | 8.5 | 40 | 1000 | 0.25 | 5 | 22.8 | 150 | 30 |
| | 33 | 7.5 | 45 | 1000 | 0.25 | 5 | 25.1 | 135 | 27 |
| | 36 | 7.0 | 50 | 1000 | 0.25 | 5 | 27.4 | 125 | 25 |
| | 39 | 6.5 | 60 | 1000 | 0.25 | 5 | 29.7 | 115 | 23 |
| | 43 | 6.0 | 70 | 1500 | 0.25 | 5 | 32.7 | 110 | 22 |
| | 47 | 5.5 | 80 | 1500 | 0.25 | 5 | 35.8 | 95 | 19 |
| | 51 | 5.0 | 95 | 1500 | 0.25 | 5 | 38.8 | 90 | 18 |
| | 56 | 4.5 | 110 | 2000 | 0.25 | 5 | 42.6 | 80 | 16 |
| | 62 | 4.0 | 125 | 2000 | 0.25 | 5 | 47.1 | 70 | 14 |
| | 68 | 3.7 | 150 | 2000 | 0.25 | 5 | 51.7 | 65 | 13 |
| | 75 | 3.3 | 175 | 2000 | 0.25 | 5 | 56.0 | 60 | 12 |
| | 82 | 3.0 | 200 | 3000 | 0.25 | 5 | 62.2 | 55 | 11 |
| | 91 | 2.8 | 250 | 3000 | 0.25 | 5 | 69.2 | 50 | 10 |
| | 100 | 2.5 | 350 | 3000 | 0.25 | 5 | 76.0 | 45 | 9.0 |

Standard Voltage Tolerance is ±10%. Add Suffix "A" for ±5% Tolerance. Other Tolerances, Non-Standard and Higher Zener Voltages Upon Request.

*Measured under thermal equilibrium and DC test conditions.

# ZENER DIODES

in MELF Package ($T_A$ = 25 °C)

| Type | Zener Voltage Range $V_Z$ at $I_{ZT}$* | Maximum Zener Impedance $Z_{ZT}$ at $I_{ZT}$ | Typical Temperature Coefficient at $I_{ZT}$ | Test Current $I_{ZT}$ | Min. Reverse Voltage at $I_R$ = 0.5 µA $V_R$ | Maximum Regulator Current $I_{ZM}$ |
|---|---|---|---|---|---|---|
| | Volts | Ohms | %/°C | mA | Volts | mA |
| | 0.65–0.75 | 8 | −0.24 | 5.0 | – | 406 |
| | 3.7–4.1 | 7 | −0.025 | 100 | – | 203 |
| | 4.0–4.6 | 7 | −0.020 | 100 | – | 182 |
| | 4.4–5.0 | 7 | −0.015 | 100 | – | 165 |
| | 4.8–5.4 | 5 | −0.005 | 100 | 0.7 | 150 |
| | 5.2–6.0 | 2 | +0.010 | 100 | 1.5 | 135 |
| | 5.8–6.6 | 2 | +0.025 | 100 | 2 | 128 |
| | 6.4–7.2 | 2 | +0.035 | 100 | 3 | 110 |
| | 7.0–7.9 | 2 | +0.035 | 100 | 5 | 100 |
| | 7.7–8.7 | 2 | +0.055 | 100 | 6 | 89 |
| | 8.5–9.6 | 4 | +0.055 | 50 | 7 | 82 |
| | 9.4–10.6 | 4 | +0.070 | 50 | 7.5 | 74 |
| | 10.4–11.6 | 7 | +0.075 | 50 | 8.5 | 66 |
| | 11.4–12.7 | 7 | +0.075 | 50 | 9.0 | 60 |
| | 12.4–14.1 | 9 | +0.075 | 50 | 10 | 55 |
| | 13.8–15.8 | 9 | +0.075 | 50 | 11 | 49 |
| | 15.3–17.1 | 10 | +0.090 | 25 | 12 | 44 |
| | 16.8–19.1 | 11 | +0.090 | 25 | 14 | 40 |
| | 18.8–21.2 | 12 | +0.090 | 25 | 15 | 36 |
| | 20.8–23.3 | 13 | +0.090 | 25 | 17 | 34 |
| | 22.8–25.6 | 14 | +0.095 | 25 | 18 | 29 |
| | 25.1–28.9 | 15 | +0.095 | 25 | 20 | 27 |
| | 28–32 | 20 | +0.095 | 25 | 22.5 | 25 |
| | 31–35 | 20 | +0.095 | 25 | 25 | 22 |
| | 34–38 | 60 | +0.095 | 10 | 27 | 20 |
| | 37–41 | 60 | +0.100 | 10 | 29 | 18 |
| | 40–46 | 80 | +0.105 | 10 | 32 | 17 |
| | 44–50 | 80 | +0.105 | 10 | 35 | 15 |
| | 48–54 | 100 | +0.105 | 10 | 38 | 14 |
| | 52–60 | 100 | +0.105 | 10 | 42 | 13 |
| | 58–66 | 130 | +0.105 | 10 | 47 | 11 |
| | 64–72 | 130 | +0.105 | 10 | 51 | 10 |
| | 70–79 | 160 | +0.105 | 10 | 56 | 9 |
| | 77–88 | 160 | +0.105 | 10 | 61 | 8 |
| | 85–96 | 250 | +0.110 | 5.0 | 68 | 7.5 |
| | 94–106 | 250 | +0.110 | 5.0 | 75 | 7 |
| | 88–110 | 300 | +0.110 | 5.0 | 75 | 7 |
| | 107–134 | 330 | +0.110 | 5.0 | 90 | 6 |
| | 130–165 | 360 | +0.110 | 5.0 | 112 | 5 |
| | 160–200 | 380 | +0.110 | 5.0 | 134 | 4 |

Standard Voltage Tolerance is ±5% for the ZMY Series and ±10% for the ZMU Series. Other Tolerances and Non-Standard Zener Voltages Upon Request. The ZMY1 is a silicon diode operated in forward direction. Hence, the cathode terminal is to be connected to the negative pole of the supply.

*Measured with pulses tp = 20 ms.

in DO-41 Package ($T_A$ = 25 °C)

| Type | Zener Voltage Range* | | Maximum Zener Impedance | | | Typical Temperature Coefficient | Maximum Reverse Leakage Current | | Surge Current (10 ms) | Maximum Regulator Current |
|---|---|---|---|---|---|---|---|---|---|---|
| | | at $I_{ZT}$ | $Z_{ZT}$ at $I_{ZT}$ | $Z_{ZK}$ at $I_{ZK}$ | $I_{ZK}$ | | $I_R$ | at $V_R$ | $I_{ZS}$ | $I_{ZM}$ |
| | $V_Z$ Volts | mA | Ohms | Ohms | mA | %/°C | µA | Volts | mA | mA |
| | 3.4–3.8 | 60 | 15 | 500 | 1 | −0.065 | 20 | 1 | 2660 | 290 |
| | 3.7–4.1 | 60 | 15 | 500 | 1 | −0.045 | 10 | 1 | 2540 | 280 |
| | 4.0–4.6 | 50 | 13 | 500 | 1 | −0.020 | 3 | 1 | 2440 | 250 |
| | 4.4–5.0 | 45 | 13 | 600 | 1 | +0.005 | 3 | 1 | 2320 | 215 |
| | 4.8–5.4 | 45 | 10 | 500 | 1 | +0.015 | 1 | 1.5 | 2200 | 200 |
| | 5.2–6.0 | 45 | 7 | 400 | 1 | +0.022 | 1 | 2 | 2080 | 190 |
| | 5.8–6.6 | 35 | 4 | 300 | 1 | +0.032 | 1 | 3 | 1960 | 170 |
| | 6.4–7.2 | 35 | 3.5 | 300 | 1 | +0.038 | 1 | 4 | 1800 | 155 |
| | 7.0–7.9 | 35 | 3 | 200 | 0.5 | +0.043 | 1 | 4.5 | 1620 | 140 |
| | 7.7–8.7 | 25 | 5 | 200 | 0.5 | +0.050 | 1 | 6.2 | 1520 | 130 |
| | 8.5–9.6 | 25 | 5 | 200 | 0.5 | +0.055 | 1 | 6.8 | 1340 | 120 |
| | 9.4–10.6 | 25 | 7 | 200 | 0.5 | +0.060 | 0.5 | 7.5 | 1200 | 105 |
| | 10.4–11.6 | 20 | 8 | 300 | 0.5 | +0.062 | 0.5 | 8.2 | 1100 | 97 |
| | 11.4–12.7 | 20 | 9 | 350 | 0.5 | +0.065 | 0.5 | 9.1 | 1000 | 88 |
| | 12.4–14.1 | 20 | 10 | 400 | 0.5 | +0.068 | 0.5 | 10 | 900 | 79 |
| | 13.8–15.6 | 15 | 15 | 500 | 0.5 | +0.072 | 0.5 | 11 | 760 | 71 |
| | 15.3–17.1 | 15 | 15 | 500 | 0.5 | +0.072 | 0.5 | 12 | 700 | 66 |
| | 16.8–19.1 | 15 | 20 | 500 | 0.5 | +0.075 | 0.5 | 13 | 600 | 62 |
| | 18.8–21.2 | 10 | 24 | 600 | 0.5 | +0.075 | 0.5 | 15 | 540 | 56 |
| | 20.8–23.3 | 10 | 25 | 600 | 0.5 | +0.078 | 0.5 | 16 | 500 | 52 |
| | 22.8–25.6 | 10 | 25 | 600 | 0.5 | +0.078 | 0.5 | 18 | 450 | 47 |
| | 25.1–28.9 | 8 | 30 | 750 | 0.25 | +0.078 | 0.5 | 20 | 400 | 41 |
| | 28–32 | 8 | 30 | 1000 | 0.25 | +0.078 | 0.5 | 22 | 380 | 36 |
| | 31–35 | 8 | 35 | 1000 | 0.25 | +0.078 | 0.5 | 24 | 350 | 33 |
| | 34–38 | 8 | 40 | 1000 | 0.25 | +0.078 | 0.5 | 27 | 320 | 30 |
| | 37–41 | 6 | 50 | 1000 | 0.25 | +0.078 | 0.5 | 30 | 296 | 28 |
| | 40–46 | 6 | 50 | 1000 | 0.25 | +0.078 | 0.5 | 33 | 270 | 26 |
| | 44–50 | 4 | 90 | 1500 | 0.25 | +0.078 | 0.5 | 36 | 246 | 23 |
| | 48–54 | 4 | 115 | 1500 | 0.25 | +0.078 | 0.5 | 39 | 226 | 21 |
| | 52–60 | 4 | 120 | 2000 | 0.25 | +0.078 | 0.5 | 43 | 208 | 19 |
| | 58–66 | 4 | 125 | 2000 | 0.25 | +0.078 | 0.5 | 47 | 186 | 16 |

Standard Voltage Tolerance is ±5%. Other Tolerances, Non-Standard and Higher Zener Voltages Upon Request.

These types are also available to specification **CECC 50005-002**.

**CECC** = Cenelec Electronic Components Committee,
**CENELEC** = European Committee for Electrotechnical Standardization.

*Measured with pulses tp = 20 ms.

# ZENER DIODES

in DO-41 Package ($T_A$ = 25 °C)

| Type | Zener Voltage Range $V_Z$ at $I_{ZT}$* | Maximum Zener Impedance $Z_{ZT}$ at $I_{ZT}$ | Typical Temperature Coefficient at $I_{ZT}$ | Test Current $I_{ZT}$ | Min. Reverse Voltage at $I_R$ = 0.5 µA $V_R$ | Maximum Regulator Current $I_{ZM}$ |
|---|---|---|---|---|---|---|
| | Volts | Ohms | %/°C | mA | Volts | mA |
| | 0.65–0.75 | 8 | –0.24 | 5.0 | – | 580 |
| | 3.7–4.1 | 7 | –0.025 | 100 | – | 290 |
| | 4.0–4.6 | 7 | –0.020 | 100 | – | 260 |
| | 4.4–5.0 | 7 | –0.015 | 100 | – | 235 |
| | 4.8–5.4 | 5 | –0.005 | 100 | 0.7 | 215 |
| | 5.2–6.0 | 2 | +0.010 | 100 | 1.5 | 193 |
| | 5.8–6.6 | 2 | +0.025 | 100 | 2 | 183 |
| | 6.4–7.2 | 2 | +0.035 | 100 | 3 | 157 |
| | 7.0–7.9 | 2 | +0.035 | 100 | 5 | 143 |
| | 7.7–8.7 | 2 | +0.055 | 100 | 6 | 127 |
| | 8.5–9.6 | 4 | +0.055 | 50 | 7 | 117 |
| | 9.4–10.6 | 4 | +0.070 | 50 | 7.5 | 105 |
| | 10.4–11.6 | 7 | +0.075 | 50 | 8.5 | 94 |
| | 11.4–12.7 | 7 | +0.075 | 50 | 9.0 | 85 |
| | 12.4–14.1 | 9 | +0.075 | 50 | 10 | 78 |
| | 13.8–15.8 | 9 | +0.075 | 50 | 11 | 70 |
| | 15.3–17.1 | 10 | +0.090 | 25 | 12 | 63 |
| | 16.8–19.1 | 11 | +0.090 | 25 | 14 | 57 |
| | 18.8–21.2 | 12 | +0.090 | 25 | 15 | 52 |
| | 20.8–23.3 | 13 | +0.090 | 25 | 17 | 48 |
| | 22.8–25.6 | 14 | +0.095 | 25 | 18 | 42 |
| | 25.1–28.9 | 15 | +0.095 | 25 | 20 | 38 |
| | 28–32 | 20 | +0.095 | 25 | 22.5 | 35 |
| | 31–35 | 20 | +0.095 | 25 | 25 | 31 |
| | 34–38 | 60 | +0.095 | 10 | 27 | 29 |
| | 37–41 | 60 | +0.100 | 10 | 29 | 26 |
| | 40–46 | 80 | +0.105 | 10 | 32 | 24 |
| | 44–50 | 80 | +0.105 | 10 | 35 | 22 |
| | 48–54 | 100 | +0.105 | 10 | 38 | 20 |
| | 52–60 | 100 | +0.105 | 10 | 42 | 18 |
| | 58–66 | 130 | +0.105 | 10 | 47 | 16 |
| | 64–72 | 130 | +0.105 | 10 | 51 | 14 |
| | 70–79 | 160 | +0.105 | 10 | 56 | 13 |
| | 77–88 | 160 | +0.105 | 10 | 61 | 12 |
| | 85–96 | 250 | +0.110 | 5.0 | 68 | 11 |
| | 94–106 | 250 | +0.110 | 5.0 | 75 | 10 |
| | 88–110 | 300 | +0.110 | 5.0 | 75 | 10 |
| | 107–134 | 330 | +0.110 | 5.0 | 90 | 8.5 |
| | 130–165 | 360 | +0.110 | 5.0 | 112 | 7.0 |
| | 160–200 | 380 | +0.110 | 5.0 | 134 | 5.5 |

Standard Voltage Tolerance is ±5% for the ZPY Series and ±10% for the ZPU Series. Other Tolerances and Non-Standard Zener Voltages Upon Request. The ZPY1 is a silicon diode operated in forward direction. Hence, the cathode terminal is to be connected to the negative pole of the supply.

*Measured with pulses tp = 20 ms.

in DO-13 Metal Case ($T_A$ = 25 °C)

| Type | Zener Voltage Range $V_Z$ at $I_{ZT}$* | Maximum Zener Impedance $Z_{ZT}$ at $I_{ZT}$ | Typical Temperature Coefficient at $I_{ZT}$ | Test Current $I_{ZT}$ | Min. Reverse Voltage at $I_R$ = 1 µA $V_R$ | Maximum Regulator Current at 45 °C $I_{ZM}$ |
|---|---|---|---|---|---|---|
| | Volts | Ohms | %/°C | mA | Volts | mA |
| | 3.7–4.1 | 7 | –0.025 | 100 | – | 240 |
| | 4.0–4.6 | 7 | –0.020 | 100 | – | 210 |
| | 4.4–5.0 | 7 | –0.015 | 100 | – | 180 |
| | 4.8–5.4 | 5 | –0.005 | 100 | – | 170 |
| | 5.2–6.0 | 2 | +0.010 | 100 | 1.5 | 160 |
| | 5.8–6.6 | 2 | +0.025 | 100 | 1.5 | 145 |
| | 6.4–7.2 | 2 | +0.035 | 100 | 2.0 | 130 |
| | 7.0–7.9 | 2 | +0.035 | 100 | 2.0 | 120 |
| | 7.7–8.7 | 2 | +0.055 | 100 | 3.5 | 110 |
| | 8.5–9.6 | 4 | +0.055 | 50 | 3.5 | 100 |
| | 9.4–10.6 | 4 | +0.070 | 50 | 5.0 | 90 |
| | 10.4–11.6 | 7 | +0.075 | 50 | 5.0 | 82 |
| | 11.4–12.7 | 7 | +0.075 | 50 | 7.0 | 75 |
| | 12.4–14.1 | 10 | +0.075 | 50 | 7.0 | 67 |
| | 13.8–15.8 | 10 | +0.075 | 50 | 10 | 60 |
| | 15.3–17.1 | 15 | +0.085 | 25 | 10 | 56 |
| | 16.8–19.1 | 15 | +0.085 | 25 | 10 | 53 |
| | 18.8–21.2 | 15 | +0.085 | 25 | 10 | 48 |
| | 20.8–23.3 | 15 | +0.085 | 25 | 12 | 44 |
| | 22.8–25.6 | 15 | +0.085 | 25 | 12 | 40 |
| | 25.1–28.9 | 15 | +0.085 | 25 | 14 | 35 |
| | 28–32 | 15 | +0.085 | 25 | 14 | 31 |
| | 31–35 | 15 | +0.085 | 25 | 17 | 28 |
| | 34–38 | 40 | +0.085 | 10 | 17 | 26 |
| | 37–41 | 40 | +0.085 | 10 | 20 | 24 |
| | 40–46 | 45 | +0.095 | 10 | 20 | 22 |
| | 44–50 | 45 | +0.095 | 10 | 24 | 20 |
| | 48–54 | 60 | +0.095 | 10 | 24 | 18 |
| | 52–60 | 60 | +0.095 | 10 | 28 | 16.5 |
| | 58–66 | 80 | +0.105 | 10 | 28 | 14 |
| | 64–72 | 80 | +0.105 | 10 | 34 | 13 |
| | 70–79 | 100 | +0.105 | 10 | 34 | 12 |
| | 77–88 | 100 | +0.105 | 10 | 41 | 11 |
| | 85–96 | 200 | +0.11 | 5 | 41 | 10 |
| | 94–106 | 200 | +0.11 | 5 | 50 | 9 |
| | 104–116 | 250 | +0.11 | 5 | 50 | 8.2 |
| | 114–127 | 250 | +0.11 | 5 | 60 | 7.5 |
| | 124–141 | 300 | +0.11 | 5 | 60 | 6.7 |
| | 138–156 | 300 | +0.11 | 5 | 75 | 6 |
| | 153–171 | 350 | +0.11 | 5 | 75 | 5.6 |
| | 168–191 | 350 | +0.11 | 5 | 90 | 5.3 |
| | 188–212 | 350 | +0.11 | 5 | 90 | 4.8 |

Standard Voltage Tolerance is ±5%. Other Tolerances and Non-Standard Zener Voltages Upon Request.

*Measured with pulses tp = 20 ms.

in Plastic Package P1 ($T_A$ = 25 °C)

| Type | Zener Voltage Range $V_Z$ at $I_{ZT}$* | Maximum Zener Impedance $Z_{ZT}$ at $I_{ZT}$ | Typical Temperature Coefficient at $I_{ZT}$ | Test Current $I_{ZT}$ | Min. Reverse Voltage at $I_R$ = 1 µA $V_R$ | Maximum Regulator Current at 45 °C $I_{ZM}$ |
|---|---|---|---|---|---|---|
| | Volts | Ohms | %/°C | mA | Volts | mA |
| | 0.71–0.82 | 1 | −0.22 | 100 | – | 1000 |
| | 3.7–4.1 | 7 | −0.025 | 100 | – | 410 |
| | 4.0–4.6 | 7 | −0.020 | 100 | – | 360 |
| | 4.4–5.0 | 7 | −0.015 | 100 | – | 330 |
| | 4.8–5.4 | 5 | −0.005 | 100 | – | 300 |
| | 5.2–6.0 | 2 | +0.010 | 100 | 1.5 | 275 |
| | 5.8–6.6 | 2 | +0.025 | 100 | 1.5 | 245 |
| | 6.4–7.2 | 2 | +0.035 | 100 | 2.0 | 220 |
| | 7.0–7.9 | 2 | +0.035 | 100 | 2.0 | 200 |
| | 7.7–8.7 | 2 | +0.055 | 100 | 3.5 | 180 |
| | 8.5–9.6 | 4 | +0.055 | 50 | 7.4 | 165 |
| | 9.4–10.6 | 4 | +0.070 | 50 | 8.2 | 145 |
| | 10.4–11.6 | 7 | +0.075 | 50 | 9.2 | 135 |
| | 11.4–12.7 | 7 | +0.075 | 50 | 10 | 120 |
| | 12.4–14.1 | 10 | +0.075 | 50 | 10.7 | 110 |
| | 13.8–15.8 | 10 | +0.075 | 50 | 12 | 98 |
| | 15.3–17.1 | 15 | +0.085 | 25 | 13.3 | 90 |
| | 16.8–19.1 | 15 | +0.085 | 25 | 14.7 | 80 |
| | 18.8–21.2 | 15 | +0.085 | 25 | 16.5 | 72 |
| | 20.8–23.3 | 15 | +0.085 | 25 | 18.3 | 66 |
| | 22.8–25.6 | 15 | +0.085 | 25 | 20.1 | 60 |
| | 25.1–28.9 | 15 | +0.085 | 25 | 22.5 | 53 |
| | 28–32 | 15 | +0.085 | 25 | 25.1 | 48 |
| | 31–35 | 15 | +0.085 | 25 | 27.8 | 44 |
| | 34–38 | 40 | +0.085 | 10 | 30.2 | 40 |
| | 37–41 | 40 | +0.085 | 10 | 29.9 | 37 |
| | 40–46 | 45 | +0.095 | 10 | 35.6 | 33 |
| | 44–50 | 45 | +0.095 | 10 | 39.2 | 30 |
| | 48–54 | 60 | +0.095 | 10 | 42.8 | 27 |
| | 52–60 | 60 | +0.095 | 10 | 47.3 | 25 |
| | 58–66 | 80 | +0.105 | 10 | 51.7 | 21 |
| | 64–72 | 80 | +0.105 | 10 | 57.1 | 20 |
| | 70–79 | 100 | +0.105 | 10 | 63.2 | 18 |
| | 77–88 | 100 | +0.105 | 10 | 68.6 | 16 |
| | 85–96 | 200 | +0.11 | 5 | 75.7 | 15 |
| | 94–106 | 200 | +0.11 | 5 | 83.7 | 13 |
| | 104–116 | 250 | +0.11 | 5 | 92.6 | 12 |
| | 114–127 | 250 | +0.11 | 5 | 101.6 | 11 |
| | 124–141 | 300 | +0.11 | 5 | 110.5 | 10 |
| | 138–156 | 300 | +0.11 | 5 | 123 | 9 |
| | 153–171 | 350 | +0.11 | 5 | 136 | 8.5 |
| | 168–191 | 350 | +0.11 | 5 | 149 | 8.0 |
| | 188–212 | 350 | +0.11 | 5 | 167 | 7.5 |

Standard Voltage Tolerance is ±5%. Other Tolerances and Non-Standard Zener Voltages Upon Request.
The ZY1 is a silicon diode operated in forward direction. Hence, the cathode terminal is to be connected to the negative pole of the supply.

These types are also available to specification **CECC 50005-18.**

**CECC** = Cenelec Electronic Components Committee,
**CENELEC** = European Committee for Electrotechnical Standardization.

*Measured with pulses tp = 20 ms.

in Metal Case ($T_A$ = 25 °C)

| Type | Zener Voltage Range | Maximum Zener Impedance | Typical Temperature Coefficient | Test Current | Min. Reverse Voltage at $I_R$ = 1 µA | Maximum Regulator Current at 45 °C | |
|---|---|---|---|---|---|---|---|
| | | | | | | without Heat Sink | with Infinite Heat Sink |
| | $V_Z$ at $I_{ZT}$* | $Z_{ZT}$ at $I_{ZT}$ | at $I_{ZT}$ | $I_{ZT}$ | $V_R$ | $I_{ZM}$ | $I_{ZM}$ |
| | Volts | Ohms | %/°C | mA | Volts | mA | mA |
| | 3.7–4.1 | 7 | −0.025 | 100 | – | 280 | 2100 |
| | 4.0–4.6 | 7 | −0.020 | 100 | – | 240 | 1750 |
| | 4.4–5.0 | 7 | −0.015 | 100 | – | 210 | 1500 |
| | 4.8–5.4 | 5 | −0.005 | 100 | – | 190 | 1430 |
| | 5.2–6.0 | 2 | +0.010 | 100 | 1.5 | 180 | 1350 |
| | 5.8–6.6 | 2 | +0.025 | 100 | 1.5 | 160 | 1250 |
| | 6.4–7.2 | 2 | +0.035 | 100 | 2.0 | 150 | 1150 |
| | 7.0–7.9 | 2 | +0.035 | 100 | 2.0 | 140 | 1060 |
| | 7.7–8.7 | 2 | +0.055 | 100 | 3.5 | 130 | 980 |
| | 8.5–9.6 | 4 | +0.055 | 50 | 3.5 | 117 | 890 |
| | 9.4–10.6 | 4 | +0.070 | 50 | 5.0 | 105 | 800 |
| | 10.4–11.6 | 7 | +0.075 | 50 | 5.0 | 95 | 710 |
| | 11.4–12.7 | 7 | +0.075 | 50 | 7.0 | 86 | 620 |
| | 12.4–14.1 | 10 | +0.075 | 50 | 7.0 | 78 | 560 |
| | 13.8–15.8 | 10 | +0.075 | 50 | 10 | 71 | 500 |
| | 15.3–17.1 | 15 | +0.085 | 25 | 10 | 65 | 465 |
| | 16.8–19.1 | 15 | +0.085 | 25 | 10 | 60 | 430 |
| | 18.8–21.2 | 15 | +0.085 | 25 | 10 | 55 | 400 |
| | 20.8–23.3 | 15 | +0.085 | 25 | 12 | 50 | 375 |
| | 22.8–25.6 | 15 | +0.085 | 25 | 12 | 45 | 345 |
| | 25.1–28.9 | 15 | +0.085 | 25 | 14 | 40 | 320 |
| | 28–32 | 15 | +0.085 | 25 | 14 | 36 | 290 |
| | 31–35 | 15 | +0.085 | 25 | 17 | 33 | 260 |
| | 34–38 | 40 | +0.085 | 10 | 17 | 30 | 235 |
| | 37–41 | 40 | +0.085 | 10 | 20 | 28 | 210 |
| | 40–46 | 45 | +0.095 | 10 | 20 | 25 | 192 |
| | 44–50 | 45 | +0.095 | 10 | 24 | 22 | 175 |
| | 48–54 | 60 | +0.095 | 10 | 24 | 20 | 162 |
| | 52–60 | 60 | +0.095 | 10 | 28 | 18.5 | 150 |
| | 58–66 | 80 | +0.105 | 10 | 28 | 17 | 137 |
| | 64–72 | 80 | +0.105 | 10 | 34 | 15.5 | 125 |
| | 70–79 | 100 | +0.105 | 10 | 34 | 14 | 112 |
| | 77–88 | 100 | +0.105 | 10 | 41 | 12.5 | 100 |
| | 85–96 | 200 | +0.11 | 5 | 41 | 11.5 | 92 |
| | 94–106 | 200 | +0.11 | 5 | 50 | 10.5 | 85 |
| | 104–116 | 250 | +0.11 | 5 | 50 | 9.5 | 77 |
| | 114–127 | 250 | +0.11 | 5 | 60 | 8.6 | 70 |
| | 124–141 | 300 | +0.11 | 5 | 60 | 7.8 | 63 |
| | 138–156 | 300 | +0.11 | 5 | 75 | 7.0 | 56 |
| | 153–171 | 350 | +0.11 | 5 | 75 | 6.3 | 51 |
| | 168–191 | 350 | +0.11 | 5 | 90 | 5.7 | 46 |
| | 188–212 | 350 | +0.11 | 5 | 90 | 5.2 | 42 |

Standard Voltage Tolerance is ±5%. Other Tolerances and Non-Standard Zener Voltages Upon Request.

*Measured with pulses tp = 20 ms.

in Plastic Package

| Type | Dwg. No. | Average Rectified Current at $T_A$ = 50 °C | Peak Inverse Voltage | Repetitive Peak Forward Current | Surge Forward Current | Conditions | Max. Forward Voltage Drop | | Max. Reverse Current | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $I_0$ Amps | P.I.V. Volts | Amps | Amps | | $V_F$ Volts * | at $I_F$ Amps | $I_R$ µA | at $V_R$ Volts |
| | P1 | 1 | 50 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 50 |
| | P1 | 1 | 100 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 100 |
| | P1 | 1 | 200 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 200 |
| | P1 | 1 | 400 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 400 |
| | P1 | 1 | 600 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 600 |
| | P1 | 1 | 800 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 800 |
| | P1 | 1 | 1000 | 10 | 50 | 8.3 ms | 1.3 | 2.0 | 5 | 1000 |
| | P1 | 1 | 1300 | 10 | 50 | 10 ms | 1.3 | 2.0 | 5 | 1300 |
| | P2 | 3 | 200 | 20 | 100 | 10 ms | 1.1 | 3.0 | 20 | 200 |
| | P2 | 3 | 400 | 20 | 100 | 10 ms | 1.1 | 3.0 | 20 | 400 |
| | P2 | 3 | 600 | 20 | 100 | 10 ms | 1.1 | 3.0 | 20 | 600 |
| | P2 | 3 | 800 | 20 | 100 | 10 ms | 1.1 | 3.0 | 20 | 800 |
| | P2 | 3 | 1300 | 20 | 100 | 10 ms | 1.1 | 3.0 | 20 | 1300 |
| | P1 | 1 | 1600 | 10 | 50 | 10 ms | 1.3 | 2.0 | 5 | 1600 |

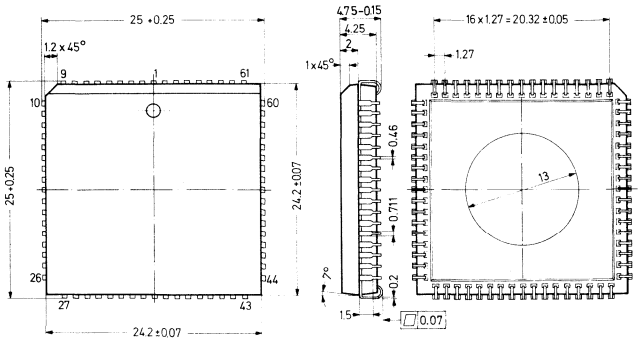
* This type is also available to British Telecom Specification D7206.

in Plastic Package

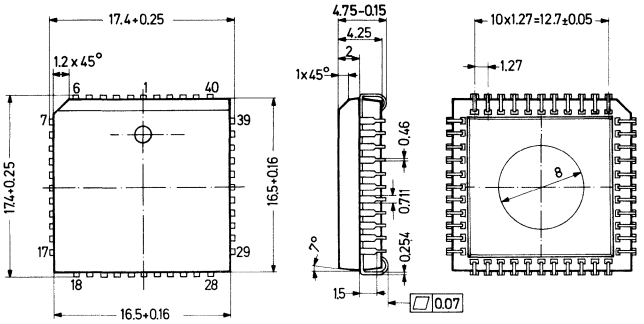
| Type | Dwg. No. | Average Rectified Current at $T_A$ = 50 °C | Peak Inverse Voltage | Surge Forward Current Half Cycle 50 Hz | Max. Forward Voltage Drop | | Max. Reverse Current | | Max. Reverse Recovery Time | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $I_0$ Amps | P.I.V. Volts | Amps | $V_F$ Volts | at $I_F$ Amps | $I_R$ µA | at $V_R$ Volts | $t_{rr}$ µs | Conditions |
| | P1 | 1 | 400 | 35 | 1.3 | 1.0 | 5 | 400 | 0.3 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P1 | 1 | 600 | 35 | 1.3 | 1.0 | 5 | 600 | 0.3 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P1 | 1 | 1000 | 35 | 1.3 | 1.0 | 5 | 1000 | 0.3 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 2 | 100 | 70 | 1.3 | 3.0 | 10 | 100 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 2 | 200 | 70 | 1.3 | 3.0 | 10 | 200 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 2 | 400 | 70 | 1.3 | 3.0 | 10 | 400 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 2 | 800 | 70 | 1.3 | 3.0 | 10 | 800 | 0.6 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 3 | 100 | 100 | 1.2 | 5.0 | 10 | 100 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 3 | 200 | 100 | 1.2 | 5.0 | 10 | 200 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 3 | 400 | 100 | 1.2 | 5.0 | 10 | 400 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |
| | P2 | 3 | 800 | 100 | 1.2 | 5.0 | 10 | 800 | 0.5 | $I_F = I_R = 10$ mA to $I_R = 1$ mA |

## All Dimensions in mm

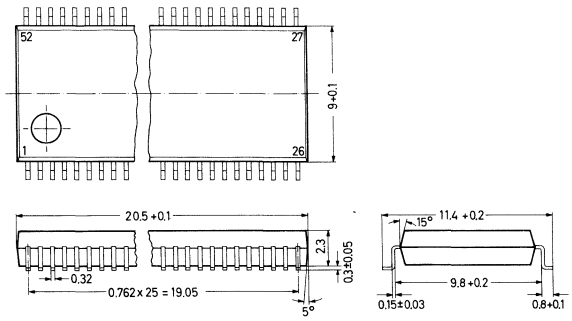
### 68-Pin PLCC Package
Weight approx. 4.5 g



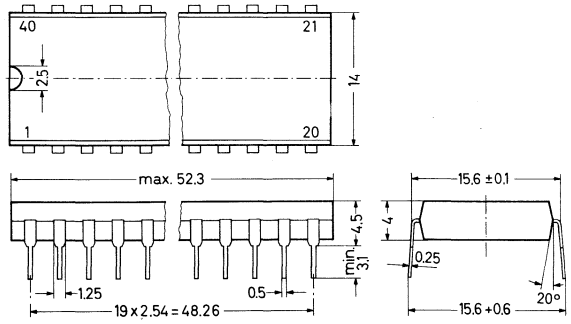

### 44-Pin PLCC Package
Weight approx. 2.2 g



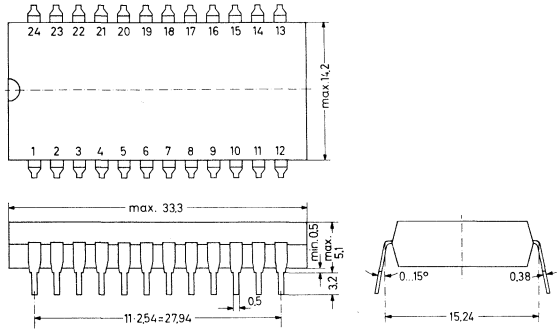

### 52-Pin Dil Plastic SMD Package
Weight approx. 0.9 g



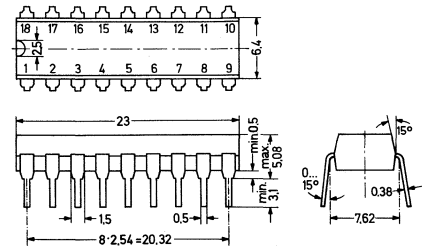

### 40-Pin Plastic Package
Weight approx. 6 g



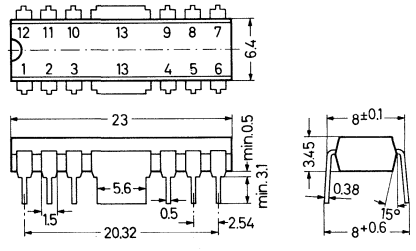

### 24-Pin Plastic Package
Weight approx. 4.5 g




### 18-Pin Plastic Package
Weight approx. 1.4 g



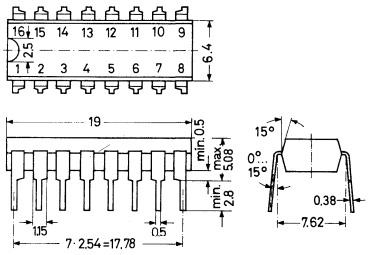

### 18-Pin Plastic Package with 2 Cooling Fins
Weight approx. 1.5 g



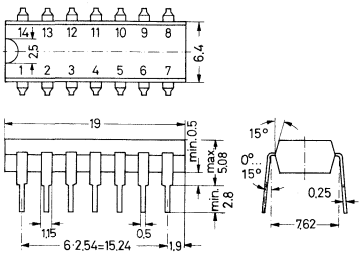
# PACKAGE OUTLINES

**All Dimensions in mm**

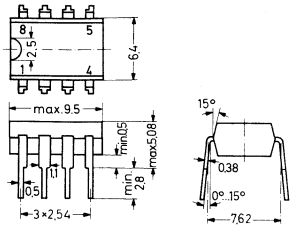
**16-Pin Plastic Package**
Weight approx. 1.1 g



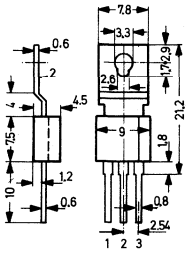

**14-Pin Plastic Package TO-116**
Weight approx. 1 g



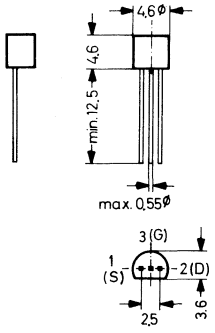

**8-Pin Plastic Package**
Weight approx. 0.5 g



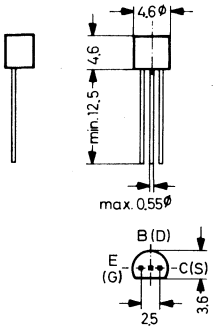

**Plastic Package TO-202**
Weight approx. 1.2 g



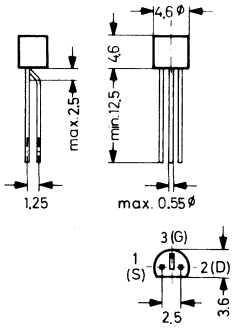

**TO-92 Plastic Package (10D3)**
Pin in-Line "A"
Weight approx. 0.18 g



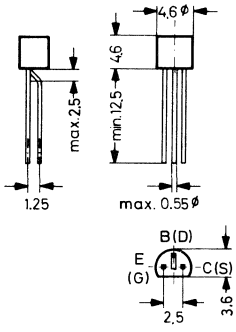

**TO-92 Plastic Package (10D3)**
Pins in-Line "B"
Weight approx. 0.18 g



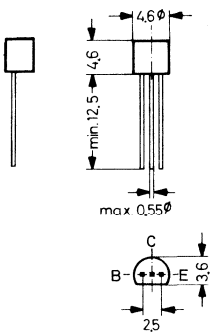

**TO-92 Plastic Package**
Pins TO-18 "A"
Weight approx. 0.18 g



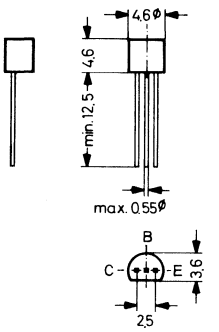

**TO-92 Plastic Package**
Pins TO-18 "B"
Weight approx. 0.18 g



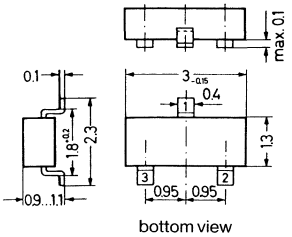

**TO-92 Plastic Package (10D3)**
Pins in-Line "D"
Weight approx. 0.18 g




**TO-92 Plastic Package (10D3)**
Pins in-Line "E"
Weight approx. 0.18 g

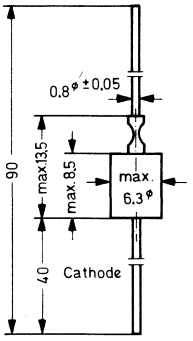



**TO-236 Plastic Package (23A3)**
Weight approx. 0.01 g

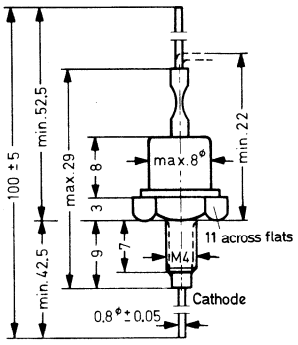


**All Dimensions in mm**

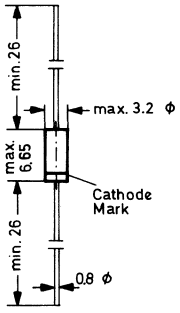
**DO-13 Metal Case**
Weight approx. 1.4 g



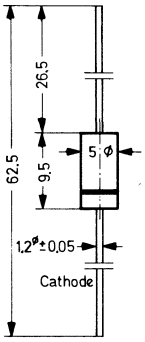

**Stud-Mounted Metal Case**
Weight approx. 6 g



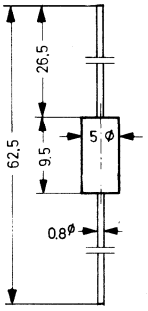

**Diode Plastic Package P1**
Weight approx. 0.4 g



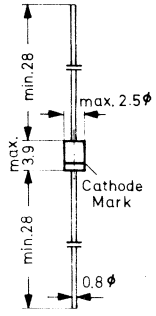

**Diode Plastic Package P2**
Weight approx. 1 g



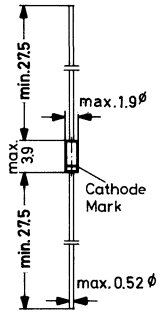

**Diode Plastic Package P3**
Weight approx. 0.6 g



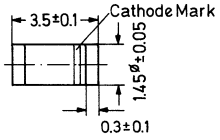

**DO-41 Glass Case**
Weight approx. 0.35 g



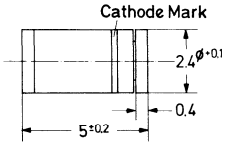

**DO-35 Glass Case**
Weight approx. 0.13 g



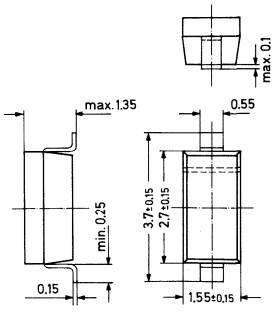

**MiniMELF Glass Case**
Weight approx. 0.05 g




**MELF Glass Case**
Weight approx. 0.25 g




**≈60A2 Diode Plastic Package**
Weight approx. 0.013 g



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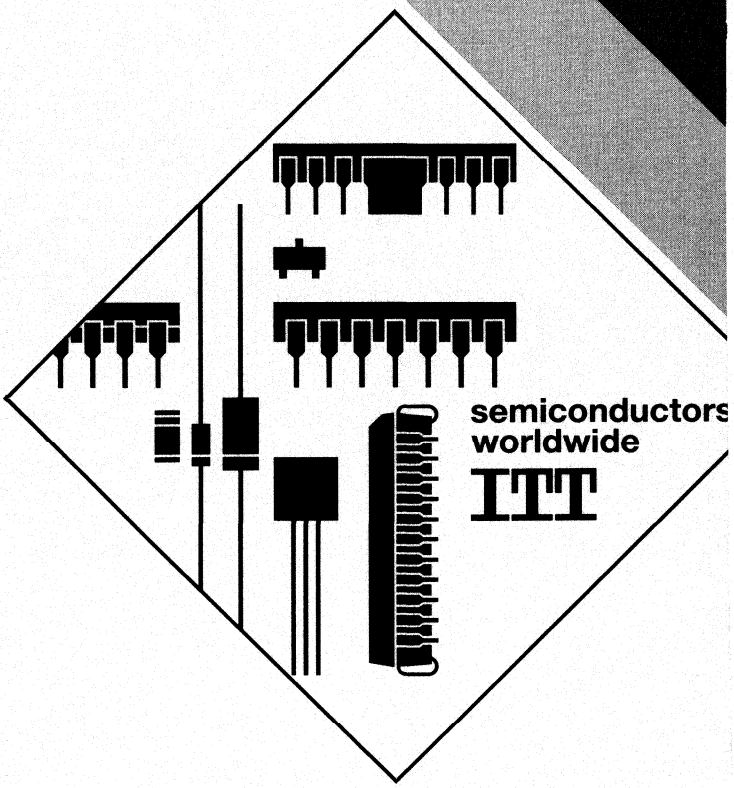


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